FINAL EXAMINATION, ECE412 FALL SEMESTER 2012

Instructions

- Lecture notes and books allowed. Use additional sheets if necessary.
- There are two questions in this exam. Only one of the problems will be counted towards your grade. If you solve more than one problem, the answer with the maximum score will be counted.
- Each question comes with hints on how to approach the problem. The hints are only suggestions and you may choose not to follow them.
- Partial credit will be provided if steps towards solving the problem are correct but the final answer is incorrect. Make sure that you indicate how you are approaching the problem.

Assumptions

- All transistors (pMOS and nMOS) have equal gate transconductance $g_m$ and drain transconductance $g_d$. The pMOS transistor is indicated by a circle at its gate.
- The wires in the diagrams are connected only where solder dots (black dots) are located.
Problem 1 (30 points)
Compute the following parameters for the circuit given below. $V_B$ is a constant bias voltage and $I_o$ is a constant bias current and $V_{dd}$ is the supply voltage:

1. Small signal gain $A_{diff} = \Delta V_{out} / (\Delta V_{in}^+ - \Delta V_{in}^-)$ [7 points]
2. Output voltage swing [4 points]
3. Power consumption [5 points]
4. Location of poles [7 points]
5. Location of zeros [7 points]
Problem 2 (30 points)
Calculate the output voltage $V_{out}$ for each of the clock phases shown below. Assume that the input voltages are constant and the opamp and the switches are ideal.