

Lab 3: Physical Design of MUX2:1 and XOR

Due: Thursday Feb. 12 2009

Summary:

Lab 3 will expose students to the design of more complex logic gates where an optimized layout can be difficult to achieve. A 2:1 MUX and 2-input XOR with built-in input signal inverters will be developed and added to the CMOS logic gate cell library.

Learning Objectives:

1. Learn to optimize the layout of complex, multi-transistor, logic gates.
2. Gain experience in designing cells to meet size objectives.
3. Become proficient with identifying and correcting DRC and LVS errors.

Estimated Time to Complete Assignment: ~6 hours plus report preparation

Resources

This lab will utilize information from all of the tutorial and guide documents from labs 1 and 2.

Procedure:

1. Create the schematic for a 2:1 multiplexer cell (MUX21) using complementary pass-gate (transmission gate) logic with minimum-sized ($L=0.6\mu\text{m}$, $W=1.5\mu\text{m}$) nMOS and pMOS transistors. See Figure 1 below and Chapter 2 notes. Include an inverter within this cell to invert the select signal. Create the inverter at the transistor level; do not instantiate an inverter cell into this schematic. You are not required to make a transmission gate cell, rather you can implement transmission gates with transistors directly within the MUX21 cell. The cell should have three inputs (e.g., a, b, s) and one output. When drawing the schematic, consider how the transistors might be arranged in the layout (step 4).
2. Create a symbol for MUX21 that looks like a MUX
3. Verify the functionality of the circuit through simulations (all possible input/output combinations).
4. Complete the cell layout for the 2:1 multiplexer and pass DRC and LVS. This cell must be designed as a primitive cell using only polygons (i.e. do not instantiate the INV cell from Lab2). Do not use Metal-2. This cell must match the $21\mu\text{m}$ pitch of all previous cells, and you should optimize the size of the cell by minimizing the cell width. You should be able to get the width of this layout close to $12\mu\text{m}$.
5. Pass DRC and LVS on the MUX21 cell.
6. A 2-input CMOS XOR (XOR2) gate was created in Lab 1. If you do not have a correctly functioning XOR2 schematic, complete this now referring back to Lab 1.
7. Construct a width-minimized layout for a static CMOS XOR2. Use the design from Lab 1; do not implement a transmission gate-based XOR. This cell must be designed as a primitive cell using only polygons (i.e. do not instantiate the INV cell from Lab2). Do not use Metal-2. Minimize the width of this cell while keeping the standard $21\mu\text{m}$ cell pitch. This can be challenging, but a main purpose of this lab is to learn how to optimize the layout of

cells with several transistors. A width of $16.8\mu\text{m}$ can be achieved following the basic primitive cell layout guidelines.

HINTS: One way to layout XOR2 is to assume the A input comes from the left and the B input comes from the right, with the input inverters at the left and right side of the cell. Also, keep in mind that Source and Drain regions can be shared between transistors (even the inverter transistors hint, hint!). When optimized, it is possible to have only one active region for the pMOS transistors and one active region for all the nMOS.

Remember to check the **Guide to Passing LVS** if you have any trouble with LVS. It contains a lot of handy tips.

8. Pass DRC and LVS on the XOR2 cell.
9. Print the Lab 3 Grading Sheet and meet briefly (~5 min.) with a TA to check off your lab by 5pm on Wednesday.
10. Construct a *Brief Report* of this assignment using the **Guide to Writing Lab Reports**. Be sure to include responses to the Discussion Topics below. Reports are due by the beginning of class on Monday but can be turned in to a TA earlier.

Deliverables:

	<i>check off</i>	<i>report</i>
Schematic and symbol of the MUX21	X	X
Functional simulation of MUX21	X	X
Layout of the MUX21 and XOR2	X	X
Widths of MUX21 and XOR2 gates		X
Results of the LVS file for each gate	X	

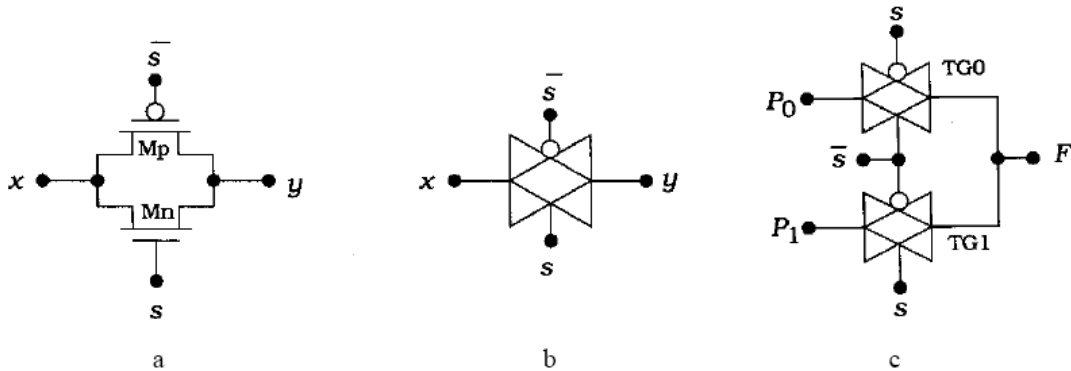


Fig. 1: (a) CMOS transmission gate, (b) transmission gate symbol, (c) 2:1 transmission-gate multiplexer, MUX21.

Discussion Topics:

Include type-written responses to the following discussion topics in your full report.

- 1. Several layout layers directly determine MOSFET parameters. a) What parameter is determined by the width of the ACTIVE layer? b) What is determined by the width of the POLY layer?*
- 2. When working with series FET transistors, what NCSU setting should be modified and why?*
- 3. A 2:1 MUX could be implemented with 2 AND logic gates and 1 NOR logic gate. How many transistors would this require for a CMOS implementation? Compare this to the number of transistors required for the transmission gate implementation.*
- 4. What layout widths (as defined in Lab 2) did you achieve for the MUX21 and XOR2 cells? Although you should have recorded this information with the Design and Results section of your full report, please include it here.*
- 5. Briefly discuss what challenges you faced in optimizing layouts, particularly with the XOR2 cell. Summarize any key discoveries that might help you optimize future cells.*