

Lab 7: Introduction to Automated Layout from Schematics

Due: Friday March 21, 2008

Summary:

This lab introduces students to automated layout methods by constructing a XOR gate and a function F using the place-and-route tools from Cadence's Encounter.

Learning Objectives:

1. How to obtain Verilog netlist file from schematic
2. How to perform place and route with Cadence's Encounter
3. How to import GDSII files into Virtuoso to generate a layout

Resources:

Tutorial PnR and files located at `/egr/courses/personal/ece410/resources/pnr`

Procedure:

1. Complete the Place-and-Route tutorial, **Tutorial PnR**, on the class website. Save or print a copy of the schematic and final layout for your check off.
 - a. While doing Tutorial PnR, you first need to create a schematic for XOR by instantiating the basic logic gates from *OSU_stdcells_ami05*. This should require INV, NAND, and NOR gates. Confirm you have this standard cell library. If not, you can copy its compressed file from `/egr/courses/personal/ece410/resources/pnr/`.
 - b. Create a Verilog netlist for the XOR schematic using the methodology in **Tutorial PnR**. Save it as a `.v` file, which is a Verilog file (e.g., XOR.v).
 - c. Place and route this netlist file with *Cadence Encounter*. Follow the procedure in the tutorial carefully. Verify geometry and connectivity to make sure there are no violations.
 - d. Import the XOR GDSII and DEF files into Virtuoso to obtain the cell layout.
2. Using logic gates from the standard cell library and following the procedure of **Tutorial PnR**, obtain an automated layout for the function $F = \overline{A \bullet B + C}$. Save or print a copy of the schematic and final layout for your check off.
3. Study the Discussion Topics below and be prepared to answer them orally with the TA during your lab check off. Note, you may need more time (10-15 min) for check off with this lab.
4. Print the Lab 7 Grading Sheet and meet with the TA to checkoff your lab by 4pm on Friday.

There is no report for this lab.

Deliverables:

Description	Check off
Schematic and layout for XOR	X
Schematic and layout for Function F	X
Verilog netlist file for XOR	X
Verilog netlist file for Function F	X

Discussion Topics:

Study the topics below and be prepared to answer them with the TA during check off.

- 1. What are the advantages and disadvantages of automatic place-and-route design versus the full custom design.*
- 2. Why is a standard cell library as OSU_stdcells_ami05 needed for place and route?*
- 3. Why does performing place and route needs a netlist file first from schematic.*
- 4. Define two of the rules for place-and-route design that you feel are most important.*
- 5. Why are Verify Geometry and Verify Connectivity necessary?*
- 6. If you wish to reload a previously-saved placed-and-routed design in Encounter, what file needs to be read in and what menu command is used to read in this file?*

Reminder: This lab should be done by each student individually; it is not a group lab.