

Lab 6: DFFR Schematic Generation and 8-bit Shift Register Design

Due: Friday March 14, 2008

Summary:

In this group lab, the last components of your custom cell library will be constructed and verified. Design techniques for “higher level” digital functional blocks using custom IC design tools are introduced and practiced by designing an 8-bit Shift Register.

Learning Objectives:

1. Gain understanding of physical design through schematic re-creation.
2. Observe the functionality of a d-type flip flop with reset.
3. Understand design hierarchy at the schematic and physical design level.
4. Observe the functionality of a digital shift register circuit.
5. Learn how to design schematics and layouts for multi-input/output bit structures.

Important Notes:

- ***This is a group lab***, to be completed by 3-person groups. Team organization and distribution of workload will be determined by individual groups. This lab is much more complex than the prior labs, so plan well, divide and conquer. It is vital that you complete steps 1 and 2 early; most subsequent steps can be done in parallel after completing those.
- Each group will submit a single report, and each student will submit an individual analysis. This is a different format than past reports. See the [Guide to Group Lab Reports](#).
- As with every layout you construct, **you must try to minimize the layout area** and keep the cells as compact as possible.

Resources:

The following documents are available on the class website to provide important information that will assist in completing this assignment.

- *dffr.tar* file located at `/egr/courses/personal/ece410/resources/`
- *Guide to Setting up Group Directories*
- *Lab 6 Supplement*
- *Guide to Multi-Cell Layout*
- *Guide to Power Measurement*
- *Guide to Group Lab Reports*

Procedure:

1. Complete the procedure described in the [Guide to Setting up Group Directories](#) to setup your group directory. The remainder of this lab is to be performed once by the group working in your group directory.
2. Construct and simulate a D flip flop with reset (DFFR)
 - a. Copy the DFFR layout (*dffr.tar*) from `/egr/courses/personal/ece410/resources/` into your group design library.

At a command prompt, go to where you saved the *dffr.tar* file and extract it by running the following command: `tar -xvf dffr.tar` Now you should have the extracted and layout views of the *dffr* cell in your group library.

- b. Generate the schematic for the provided DFFR cell by mapping the layout to a schematic. **The schematic must be made at the transistor level; no gate symbols can be used.** See the *Guide to Designing CMOS Flip Flops* in **Lab 6 Supplement** for helpful information.
 - c. Pass LVS and save your schematic.
 - d. Create a symbol for the DFFR cell.
 - e. Verify the functionality of the DFFR cell with simulations. Try to show all possible logic cases including asynchronous reset in one simulation plot. Measure the “clock to Q” time for both rising and falling output. Read *Discussion Topic 1* before continuing.
3. Construct a 4:1 multiplexer using instances of the 2:1 multiplexer designed in a previous lab. Create a schematic, a symbol, and a layout that passes DRC and LVS. You must maintain a hierarchical design structure by instantiating (not copying) lower level cells. See the **Guide to Multi-cell Layout** for additional tips. Verify functionality with simulations. Read *Discussion Topic 2* before continuing.
 4. Using DFFR and multiplexer cells, construct an 8-bit shift register that can implement the truth table given here. Refer to class notes and the **Lab 6 Supplement** document.

S2	S1	S0	Function
0	0	X	Parallel Load
0	1	0	Shift Right
0	1	1	Rotate Right
1	0	0	Shift Left
1	0	1	Rotate Left
1	1	X	Set (data output bits go to 1)
X	X	X	Reset (when Reset = 1, all data outputs go to 0)

 - a. Complete the schematic and verify proper functional operation using schematic-level simulations. You do not need to include these in your report, but you should not begin the next step until you know ALL FUNCTIONS of the shift register are working correctly. Use a clock of 50MHz.
 - b. Construct the layout of the 8-bit shift register placing all cells in a single row with the same power supply rails. Pass DRC and LVS. Before extracting, remember to run the command `NCSU_parasiticCapIgnoreThreshold=1e-18` in the Command Interpreter Window to include the parasitic capacitances in the extracted view.
 - c. Complete post-layout simulation for the shift register with CLK at 50MHz. Simulate all functions in the truth table and determine the slowest function. Do a final simulation of this function to show in your report. Perform a parallel reset of all 8 bits at the beginning of your simulation and measure the worst-case delays (propagation & rise/fall times) for the slowest function of the cell. If necessary, refer back to Tutorial C for post layout simulation guidelines. You do not need to report the timing for all functions, just the one with the critical path delay. Read *Discussion Topic 3* before continuing.
 5. Review the **Guide to Power Measurement** and measure the following for *extracted views* the DFFR cell and the Shift Register: 1) static power dissipation, 2) dynamic power dissipation, 3) total average power dissipation. Note the guide has more information than you need to complete this step; the other material is just for your reference. For the DFFR cell, use a simulation with a 50MHz clock and toggle the D input high and low for two cycles at 20MHz (i.e., run simulation for 100n). For the Shift Register cell, use your worst-

case delay simulation. To avoid unpredictable start-up states, toggle the *reset* line at the beginning of your simulations (initiate *reset* to low and immediately pull it high).

6. {Do this step for Extra Credit only; it is not required} Using the DFFR cell, construct the schematic for an asynchronous counter that can count to eight (0-7). Perform a schematic-level simulation that verifies counting over 10 input cycles. Include the plot in your report and use handwritten annotations to clarify proper operation.
7. Print the Lab 6 Grading Sheet and check off your lab with a TA by 4pm on Friday. Only one person from your group is required for check off.
8. Prepare a **Group Report** of this assignment using the **Guide to Writing Group Lab Reports**. Include requested data within the appropriate sub-sections of your report, and be sure to include responses to the *Discussion Topics* below. Remember that in addition to the group report, each student needs to prepare an *Individual Analysis*. Reports are due by the beginning of class on Monday. The *Individual Analysis* reports will be kept confidential.

Deliverables:

		<i>check off</i>	<i>lab report</i>
1	Schematic for the DFFR cell	X	X
2	Post-layout simulation graphs and specified results for DFFR		X
3	Schematics and layouts for 4:1MUX	X	X
4	Schematic and layout of the 8-bit Shift Register	X	X
5	LVS results for DFFR and 8-bit Shift Register	X	
6	Post-layout simulation graphs and specified results for Shift Register		X
7	Power measurements		X
8	{Extra Credit} Schematic of 0-7 asynchronous counter	X	X
9	{Extra Credit} Simulation results for 0-7 asynchronous counter		X

Discussion Topics

Include type-written responses to the following discussion topics in your brief report.

1. *Is the DFFR a positive-edge-triggered or negative-edge-triggered FF? Briefly describe the hold time for a d-type flip flop and estimate its value.*
2. *Briefly define two of the rules for multi-cell layout that you feel are most important.*
3. *Briefly discuss the worst-case function of the shift register. Is it what you expected? Why or why not?*
4. *Briefly discuss the pros and cons of the asynchronous counter versus a synchronous counter. Answer this question even if you did not complete the extra credit step.*