

Lab 5: Introduction to Parametric Analysis

Due: Friday February 29, 2008

Summary:

Lab 6 introduces the use of simulation tools to perform parametric analysis, wherein designers can observe the impact of varying specific circuit/device parameters.

Learning Objectives:

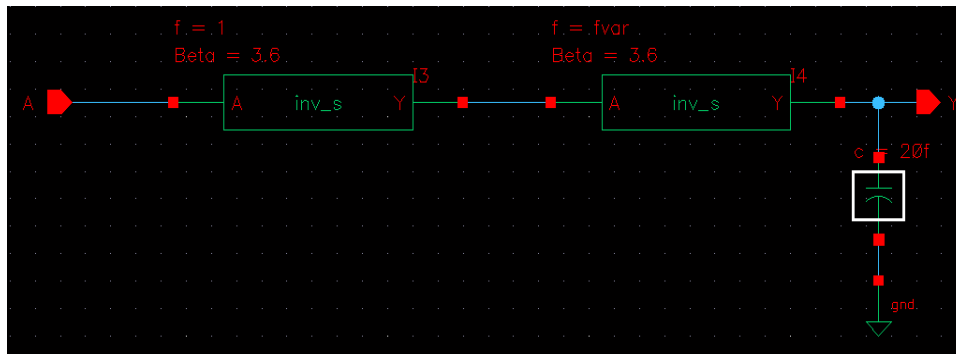
1. Learn how to use and set design variables and how to create cells that use passed parameters.
2. Learn how to perform parametric analysis and use it to solve a simple optimization problem.
3. Observe the effect of varying transistor widths on the delays of an inverter and the effect of varying input voltage slope on inverter delays.

Resources: *Tutorial D***Preliminary Notes:**

To ensure consistency of results, always use a 3V square wave with a rise and fall time of 0.05ns as the input to your inverter unless otherwise specified by the instructions. A width of 5ns and a period of 10ns are recommended, but may be any values that allow the output to fully rise and fall.

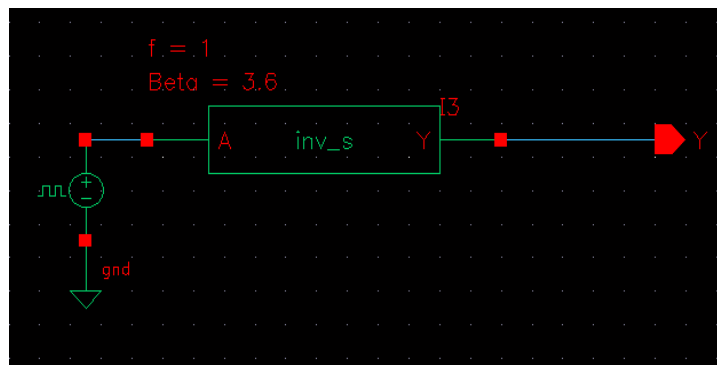
Procedure:

1. Complete [Tutorial D](#). Before continuing, be sure you have a good understanding of the following concepts: specifying and setting design variables and passed parameters, and parametric analysis.
2. Construct and analyze an inverter with equal high-to-low and low-to-high propagation delays.
 - a. Using parametric analysis on an inverter schematic, determine the approximate Wp/Wn ratio that equalizes the propagation low-to-high (LH) and propagation high-to-low (HL) delays. You must choose a value that will result in a PMOS width that is multiple of $\lambda/2$ (0.15 μm). Record the value of Wp/Wn, t_{HL} , t_{LH} , and calculate the percentage difference in the two times ($|\text{difference}/\text{average}|$). Save the plot showing the inverter propagation delays for the β that equalizes t_{HL} and t_{LH} . Refer to this Wp/Wn value as the “measured β value” for the rest of the assignment.
 - b. Create a new inverter layout with the PMOS width changed to match the measured β value. Extract the layout (including parasitic capacitances) and run transient simulation using the extracted view. Use the same input stimulus file that you used in Step 2. Record the propagation HL, propagation LH delays, and calculate the percentage difference in the two times. Save the plot showing the inverter propagation delays from the extracted view.
 - c. Create a new inverter cell that uses the following two passed parameters: “Beta” and “f” (inverter size). “Beta” should be used as a multiplier for the PMOS transistor width, and “f” should be used as a multiplier for both the PMOS and the NMOS widths. In other words, the width of the PMOS will be the product of “Beta”, “f”, and the specified minimum width 1.5 μm , and the width of the NMOS will be the product of “f” and the specified minimum width 1.5 μm .
 - d. Create a new symbol for the new inverter. If you use a copied symbol, you will not be able to pass parameters to it. The symbol shape may be left as the default box.
3. Determine how to set transistor sizes to minimize output transition delays.
 - a. Create a new schematic. Place two of these new inverters in series, followed by a 20f F capacitor. For both inverters, pass the “measured β ” value that you determined in step 2. For the first inverter, pass an “f” value of 1. Parameterize the passed value for “f” of the second inverter. Your schematic should look similar to the following figure:



Note: Beta value was picked at random in this example. The red text above the symbols does not appear by default. The shape of the inverter symbol does not matter here.

- b. Using parametric analysis, determine the value of “f” for the second inverter that minimizes the end-to-end propagation delay (from the input of the first inverter to the output of the second inverter) in the circuit. Limit the range of “f” to between 1 and 3. The measurement should be to the nearest tenth (0.1). Do not worry if this “f” value results in transistor widths that are not multiples of $\lambda/2$ (0.15 μm). Record this value of “f” and the corresponding propagation LH and HL delays. Save the plot showing the inverter propagation HL and LH delays for the optimal value of “f”.
4. Analyze the effect of input rise and fall times on output transition delays.
- a. Create a new schematic. Place a pulse voltage source followed by the new inverter using your measured β value and an “f” value of 1. Specify a 3V voltage pulse with a 5ns width, 10ns period, and parameterized rise and fall times. The rise and fall times should be set using the **same design variable name**, so that they are identical. Your schematic should look similar to the following figure:



- b. Using parametric analysis, sweep the voltage pulse rise/fall time from 0.05n to 0.50n in 11 linear steps. Record the average inverter propagation delay (the **average** of propagation HL and LH delays) for each of the 11 different input transition times.

Note: Do not include an input voltage source in your stimulus file here. It is only necessary to set vdd to 3V.

- c. Plot inverter propagation delay vs. inverter input rise/fall time using a program like Excel, Mathematica or MATLAB. Make sure the data is connected by lines – either point-to-point, or using a fitted line. This step can be performed after completing the lab assignment.
- d. Find the line of best fit (i.e. slope and y-intercept) for the inverter propagation delay vs. input rise/fall time using a simple linear regression. In Excel, this can be accomplished by using the SLOPE and INTERCEPT functions on the data.

5. Build a schematic for a two-input AND gate by instantiating your previously-designed NAND gate followed by the new parameterized inverter cell. Pass the measured β value and an “f” value of 1 to the inverter. It is not necessary to make a symbol or layout. Simulate the AND gate for a 11 \rightarrow 10 falling transition and measure the propagation delay.
 - a. Using the results from your linear regression in step 4d and the timing analysis for the NAND done previously in Lab 5, calculate the predicted 11 \rightarrow 10 falling propagation delay for the AND gate. Compare this to the measured value by calculating the % error. It is not unreasonable to have high accuracy here, assuming you have carefully measured all necessary delays and have done the calculations correctly.
6. Print the Lab 6 Grading Sheet and check off your lab with a TA by 4pm on Friday.
7. Construct a report of this assignment using the [Guide to Writing Lab Reports](#). **Include appropriate tables or lists of all data collected during this lab** that clearly identify what data is presented. Be sure to include responses to the Discussion Topics below. Reports are due by the beginning of class on Monday.

Deliverables:

		<i>check off</i>	<i>lab report</i>
1	Measured β , t_{HL} , t_{LH} , and % difference from parametric analysis of INV		X
2	Plot of inverter simulation using measured β , from schematic	X	X
3	Layout of inverter sized for measured β	X	X
4	Measured rise time, fall time, and % diff from layout-extracted INV		X
5	Plot of inverter simulation using measured β , from extracted	X	X
6	Measured INV size “f” that optimizes end-to-end delay		X
7	Plot showing propagation delay of the two-inverter chain for optimal sizing “f”	X	X
8	Data series for inverter propagation delay vs. input rise/fall time	X	X
9	Plots of inverter propagation delay vs. input voltage rise/fall time		X
10	Line of best fit for propagation delay vs. input voltage rise/fall time		X
11	Measured and calculated propagation delay for 11 \rightarrow 10 transition in AND gate, along with % error of calculation		X

Discussion Topics

Include type-written responses to the following discussion topics in your brief report.

1. Discuss the benefits and drawbacks of using a W_p/W_n that equalizes propagation HL and LH delays for an INV. Will this W_p/W_n result in an optimal propagation delay (assuming the NMOS width is minimum)?
2. Using the measured β value, what could account for any difference in the inverter propagation delays measured from a) simulations of the schematic and b) simulations of the extracted view.
3. Why is it necessary to specify transistor dimensions that are in multiples of $0.15\mu\text{m}$ when simulating from the schematic in Step 2?
4. When considering the size of the second inverter in the two-inverter chain with a load capacitance, why is there an optimal solution for the delay? In other words, why does the delay begin to increase for increasing inverter sizes?
5. Why does increasing the magnitude of the input voltage rise/fall time (i.e. slope) increase the propagation delays and rise/fall times of the inverter?