

Lab 2: Introduction to CMOS Physical Design

Check Off by Friday Feb 1st

Summary:

Lab 2 introduces the CMOS physical design process by designing a CMOS Inverter, NAND, and NOR using Cadence Virtuoso Layout Editor. Students will create the physical layout for cells created in Lab1 and learn about Design Rules Check and Layout vs. Schematic comparison.

Learning Objectives:

1. Learn about various layers in CMOS physical design and become familiar with design rules for each layer.
2. Learn to use Virtuoso Layout Editor
3. Understand the physical design of CMOS inverter, NAND, and NOR gates.
4. Discover how to optimize layouts by creating minimum width designs for gates. Only the most compact designs will receive full points (Hint: You can share source/drain regions).

Resources: This lab uses *Tutorial B, Guide to Primitive Cell Layout* and *Guide to Passing LVS* on the ECE410 website.

Estimated Time to Complete Assignment: 5-6 hours

Procedure:

For this lab, you should follow the steps described in Tutorial B to create the layout for an inverter and 2-input NAND and NOR gates using minimum-sized transistors for the AMI C5N fabrication process.

1. Read the [Guide to Primitive Cell Layout](#) and familiarize yourself with the cell layout guidelines.
2. Follow the steps in [Tutorial B](#) to construct the layout for a CMOS Inverter cell using minimum-sized ($L=0.6\mu\text{m}$, $W=1.5\mu\text{m}$) nMOS and pMOS transistors.
3. Using [Tutorial B](#), perform Design Rule Check to make sure that your layout does not have any design rule violations. Fix any errors and repeat DRC until no errors are found.
4. Using [Tutorial B](#), extract the circuit from the layout and perform LVS. If there are any LVS errors, see the [Guide to Passing LVS](#) for suggestions on how to fix them. Note: an error-free LVS output file will be about 10-15 lines of text and should contain the words “*the netlists match*”. When LVS is correct, save the LVS results file in your working directory using a name specific to the cell you are working on so you can show it to a TA during check off.
5. Follow steps 2-4 to complete the layout for a CMOS NAND gate. While maintaining the same pitch as the inverter cell, optimize the layout to have the minimum possible width. Pass DRC and LVS and save the LVS report to show a TA during check off.
6. Measure and record width of NAND layout cell (measure the vdd/gnd rail from left to right). This information will be reported in the Discussion Topics section of your report.
7. Repeat steps 5 and 6 to complete the layout for a CMOS NOR gate, passing DRC and LVS, saving the LVS report, and measuring the cell width.

8. Print the Lab 2 Grading Sheet and meet briefly (~5 min.) with a TA to check off your lab by 4pm on Friday.
9. Construct a *Brief Report* of this assignment using the [Guide to Writing Lab Reports](#). Be sure to include responses to the Discussion Topics below. The report will be graded by a TA for 15 of the 20 points for this lab assignment. Brief Report are due by the beginning of class on Monday but can be turned in to a TA earlier.

Deliverables:

The following items must be shown to a TA during the check off procedure and/or included in your report of this lab assignment.

		<i>check off</i>	<i>report</i>
1	Layout of the CMOS Inverter, NAND and NOR gates.	X	X
2	Widths of NAND and NOR gates		X
3	Result of the LVS file for each gate.	X	

Discussion Topics:

Include type-written responses to the following discussion topics in your brief report.

1. *What is cell “pitch” and what is the value for the pitch of the cells in this lab?*
2. *Which layers are allowed to extend beyond the “boundary” of a layout cell?*
3. *What are the two primary rules for placing ports in a layout?*
4. *What are the widths of the NAND and NOR layouts in this lab?*
5. *Comment on the relative size of the NAND and NOR layouts. If they are the same, why? If they are different, why?*
6. *Describe briefly in your own words what DRC is and why it is important.*
7. *Describe briefly in your own words what LVS is and why it is important.*