

Problem 1

- In Cadence, construct the schematic for a 6T SRAM cell with all transistors minimum sized.
- Setup a stimulus file wherein *bit* is initialized to ground and *bit_bar* to VDD. Then switch *bit* to VDD and *bit_bar* to ground where they will remain. Connect the *wordline* to a voltage source that switches from low to high after the final bit/bit_bar values are set. Measure the rise time of the internal node connected to *bit* through the access transistor. Record this value as the SRAM write delay.
- Check the fall time of the other internal node (connect to *bit_bar*) when *wordline* is turned on and comment on any differences in this value and that from part (b). What circuit parameter could you change to make these values match?
- Increase the size of both access transistors by a factor of two and repeat parts (b) and (c). Comment on the differences in the SRAM write delay for two different access transistor sizes.

Problem 2

The storage capacitor in a DRAM has a value of $C_s = 75\text{fF}$. The circuitry restricts the capacitor voltage to a value of $V_{\text{max}} = 2.5\text{ V}$. When the access transistor is off, the leakage current of the cell is estimated to be 5nA .

- How many electrons can be stored on C_s ?
- How many fundamental charge units q leave the cell in 0.1 second due to leakage current?
- Calculate the time needed to completely discharge the storage capacitor through leakage current.

Problem 3

Consider a DRAM cell that has a storage $C_s=75\text{fF}$, $V_{\text{dd}}=3.0\text{V}$, and $V_{\text{th}}=0.65\text{V}$. The leakage current from the storage capacitor is estimated to be 500pA . The capacitor has a voltage V_{max} across it when the word line is brought low at time $t=0$.

- Calculate the time it takes to discharge the capacitor to 1.0V .
- Assuming the leakage current is constant for all values of storage capacitor voltage and that the minimum readable stored voltage is 1V , plot the DRAM hold time as a function of leakage current.
- From your plot, estimate the maximum leakage allowed for a hold time of 1msec .
- What is the required refresh rate for the conditions in part (c)?
- Assuming that $V_s = 2.5\text{V}$, what is the maximum bit-line capacitance, C_{bit} , that will provide a logic high output to be read with at least 0.25V on the bit line?

Problem 4

Draw the schematic for a circuit that will ensure an SRAM with two write ports is never written by both inputs at the same time. If both writeline signals are active, your circuit should either disable both or allow only one to write (prioritized).

Problem 5

Sketch the transistor-level schematics for the following basic logic gates using domino logic (not static CMOS): INV, AND, OR, XOR.