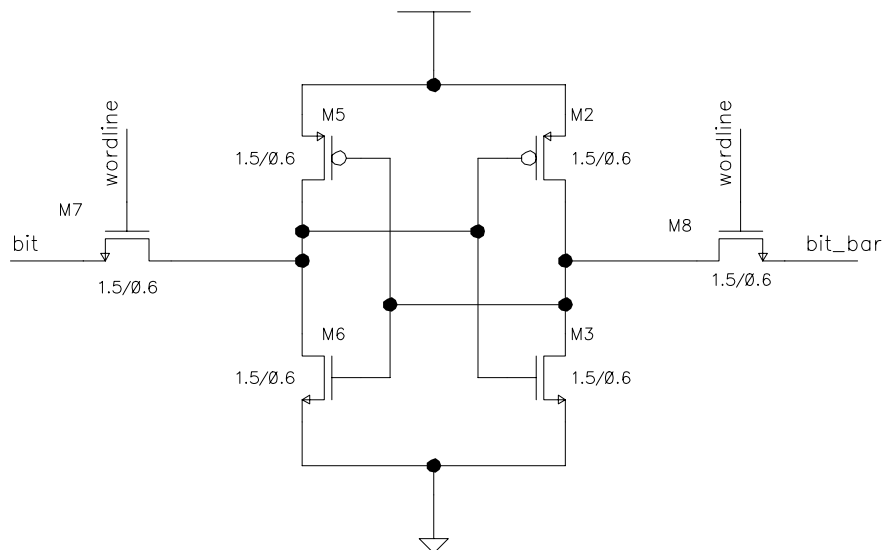


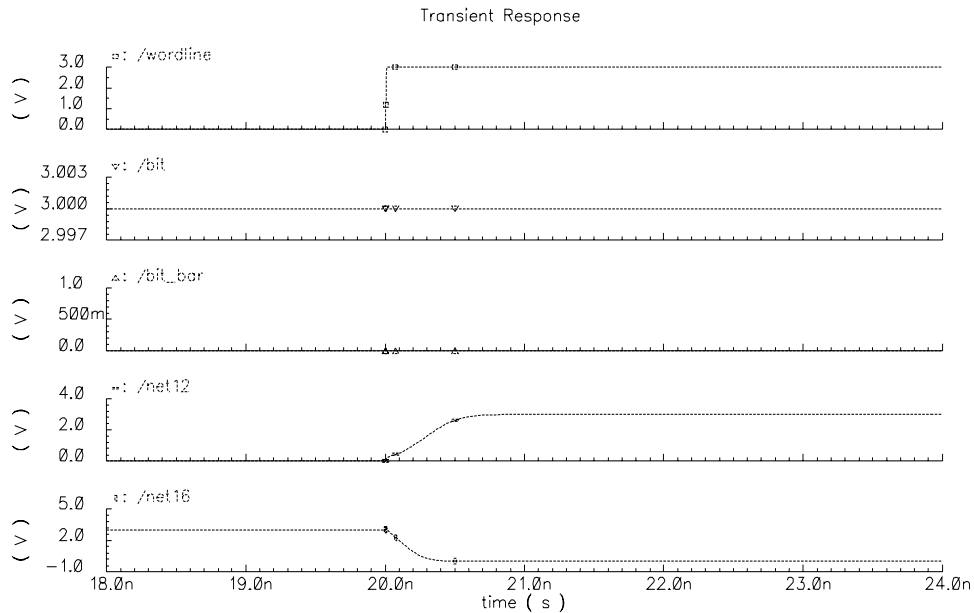
Problem 1

- In Cadence, construct the schematic for a 6T SRAM cell with all transistors minimum sized.
- Setup a stimulus file wherein *bit* is initialized to ground and *bit_bar* to VDD. Then switch *bit* to VDD and *bit_bar* to ground where they will remain. Connect the *wordline* to a voltage source that switches from low to high after the final bit/bit_bar values are set. Measure the rise time of the internal node connected to *bit* through the access transistor. Record this value as the SRAM write delay.
- Check the fall time of the other internal node (connect to *bit_bar*) when *wordline* is turned on and comment on any differences in this value and that from part (b). What circuit parameter could you change to make these values match?
- Increase the size of both access transistors by a factor of two and repeat parts (b) and (c). Comment on the differences in the SRAM write delay for two different access transistor sizes.

Solution

- The schematic and simulated waveform for a 6T SRAM cell are shown below. Simulated SRAM write delay is 0.5ns.
- Fall time of the other internal node is 0.25ns. This time is much smaller than the write delay because an NMOS switch has less channel resistance for passing a '0' than for passing a '1'. We can increase aspect ratio of the access transistor connected to *bit* signal to make the values match.
- With the width of both access transistors doubled, write delay and fall time of the other internal node reduce to 0.38ns and 0.09ns, respectively. The two values are different due to the same reason as that described in part (b). Compared with previous design, SRAM write delay is decreased by 24% due to reducing the resistance of the access transistor which allows the input voltage to drop more across the SRAM transistor than the access transistor.





Problem 2

The storage capacitor in a DRAM has a value of $C_S = 75\text{fF}$. The circuitry restricts the capacitor voltage to a value of $V_{\text{max}} = 2.5\text{ V}$. When the access transistor is off, the leakage current of the cell is estimated to be 5 nA .

- How many electrons can be stored on C_S ?
- How many fundamental charge units q leave the cell in 0.1 second due to leakage current?
- Calculate the time needed to completely discharge the storage capacitor through leakage current.

Solution

a) $Q_{\text{max}} = C_S V_{\text{max}} = 75\text{f} (2.5) = 187.5\text{f} = 1.88 \times 10^{-13}\text{ C}$

Because the charge in coulombs of a single charge unit $q = 1.6 \times 10^{-19}$,

$\#q = Q_{\text{max}}/q = 1.88 \times 10^{-13}/1.6 \times 10^{-19} = \underline{1.18 \times 10^6}$

b) Since $I = \Delta Q/\Delta t$ and the leakage current is 5 nA ,

$\Delta Q = I \cdot \Delta t = 5\text{ n} (0.1) = 5 \times 10^{-10}\text{ C}$

Because the charge in coulombs of a single charge unit $q = 1.6 \times 10^{-19}$,

$\#q = \Delta Q/q = 5 \times 10^{-10}/1.6 \times 10^{-19} = \underline{3.125 \times 10^9}$

which is 3 orders magnitude more than the charge stored on C_S (see part a)

c) $I_L = \Delta Q/\Delta t \rightarrow I_L = Q_{\text{max}}/t_{\text{max}} \rightarrow t_{\text{max}} = Q_{\text{max}}/I_L = 1.88 \times 10^{-13}/5 \times 10^{-9}$

$t_{\text{max}} = 3.76 \times 10^{-5}\text{ sec} = 37.6\text{ }\mu\text{s}$

Problem 3

Consider a DRAM cell that has a storage $C_s=75\text{fF}$, $V_{dd}=3.0\text{V}$, and $V_{th}=0.65\text{V}$. The leakage current from the storage capacitor is estimated to be 500pA . The capacitor has a voltage V_{max} across it when the word line is brought low at time $t=0$.

- Calculate the time it takes to discharge the capacitor to 1.0V .
- Assuming the leakage current is constant for all values of storage capacitor voltage and that the minimum readable stored voltage is 1V , plot the DRAM hold time as a function of leakage current.
- From your plot, estimate the maximum leakage allowed for a hold time of 1msec .
- What is the required refresh rate for the conditions in part (c)?
- Assuming that $V_s = 2.5\text{V}$, what is the maximum bit-line capacitance, C_{bit} , that will provide a logic high output to be read with at least 0.25V on the bit line?

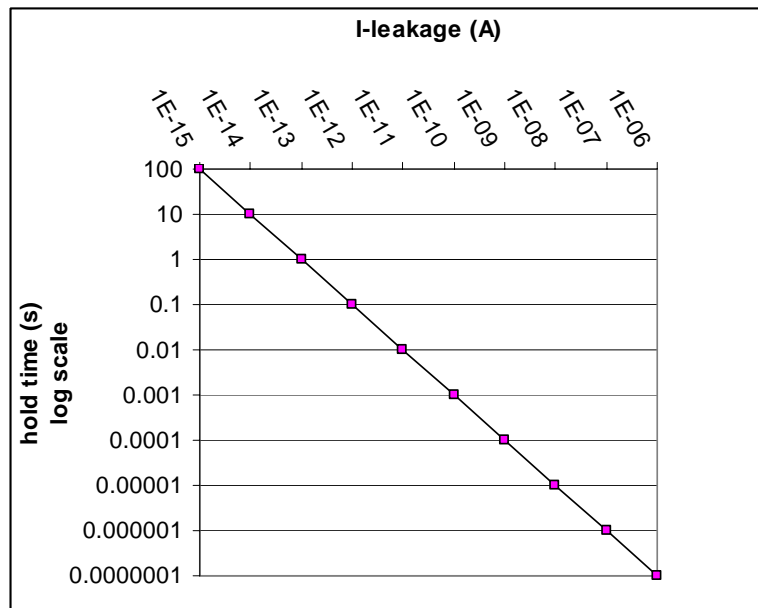
Solution

a) The time needed to discharge the capacitor to $V_{new}=1.0\text{V}$ is:

$$t = \frac{C_s(V_{max} - V_{new})}{I_L} = \frac{C_s(V_{dd} - V_{th} - V_{new})}{I_L} = \frac{75 * 10^{-15} (3 - 0.65 - 1.0)}{5 * 10^{-10}} = 202.5 \mu\text{s}$$

b) Assuming constant leakage current, we can express the DRAM hold time as a function of leakage current:

$$t_H = \frac{C_s(V_{max} - V_{new})}{I_L} = \frac{C_s(V_{dd} - V_{th} - V_{new})}{I_L} = \frac{75 * 10^{-15} (3 - 0.65 - 1.0)}{I_L} = \frac{101.25 * 10^{-15}}{I_L} \approx \frac{10^{-13}}{I_L} \text{ s}$$



c) From the plot, $I = 10^{-10} = 100\text{pA}$

d) The required refresh rate is

$$f_{refresh} = \frac{1}{2t_H} = \frac{1}{2 * 1 * 10^{-3}} = 500s^{-1}$$

e) Cbit equals the bit-line capacitance needed to maintain a voltage of $V_f = 0.25$ on the bit line. Total available charge $C_s V_s$ is redistributed over $C_s + C_{bit}$ reducing voltage to V_f , so $C_s V_s = V_f (C_s + C_{bit})$. Therefore,

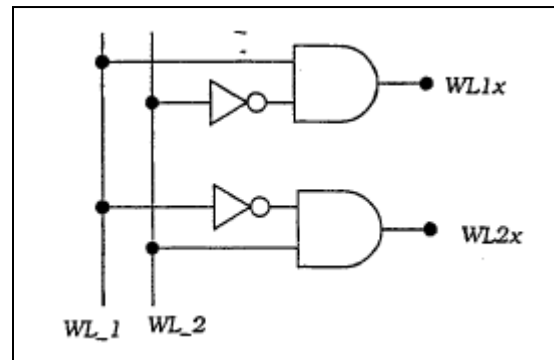
$$C_{bit} = C_s \left(\frac{V_s}{V_f} - 1 \right) = 75 * 10^{-15} \left(\frac{2.5}{0.25} - 1 \right) = 675 fF$$

Problem 4

Draw the schematic for a circuit that will ensure an SRAM with two write ports is never written by both inputs at the same time. If both writeline signals are active, your circuit should either disable both or allow only one to write (prioritized).

Solution

There may be many possible solutions to this open-ended design problem. The following circuit will ensure that, if one WL is high, the other will be low. If both are high, both output WL_x 's will be low and no data will be written.



Problem 5

Sketch the transistor-level schematics for the following basic logic gates using domino logic (not static CMOS): INV, AND, OR, XOR.

Solution:

Schematics are below. Notice an INV gate can not be created strictly following the domino logic structure, but a 2-inverter buffer can generate a reasonable solution. Other configurations may also be acceptable. For the XOR, the internal nMOS network generates the XNOR function.

