ECE 410 **Homework 8** **Spring 2008**

Due Monday March 31, 2008

Problem 1

a) Complete the following truth table for a 4-bit shift left/right circuit that specifies the number of bits to shift by the 2-bit word SH and the direction of shift by the 1-bit R/L signal (R/L=1 denotes shift right, R/L=0 denotes shift left). Assume the original data is a0-a3 and complete the table by assigning which value, a0-a3, should be at each output for each input combination.

SH		R/L	f3	f2	f1	f0
0	0	0	a3	a2	a1	a0
0	1	0				
1	0	0				
1	1	0				
0	0	1				
0	1	1				
1	0	1				
1	1	1				

b) Are there any redundant cases, and if so which ones?

c) If this were a rotate rather than a shift would you expect redundant cases and if so which ones?

Problem 2

Use Cadence tools to construct a schematic for a 3-bit Carry Look-Ahead adder. Use the circuits shown in Figure 12.18 of your textbook as the basis for creating the carry terms and build the full pseudo nMOS version of these circuits to generate the carry terms. To complete the 3b adder circuit you may instantiate the INV, NAND, NOR, and XOR gates you have previously designed. Your inputs should be a0, a1, a2, b0, b1, b2, and c0, and your outputs should be s0, s1, s2, c1, c2, and c3. Use minimum sized transistors for the nMOS network but size the pMOS load transistors at W/L=1.5/3.2 to provide a reasonable rise time and output low voltage. Your homework paper should include the complete schematic.

Problem 3

Simulate the 3b CLA adder for the following inputs

case A. a: 0 0 1
b: 0 0 1
c0: 0

case B. a: 0 1 0
b: 1 0 1
c0: 0

case C. a: 1 1 1
b: 0 0 0
c0: 1

Force the inputs to all change at the same time, plot the outputs s0, s1, s2, and c3 for each of the above cases and show these results in your homework paper. Report the delay time from input set until the last (slowest) output is set. Describe the addition function for each of the above cases in decimal numbers and show that the addition was correct.