

Problem 1

2-input CMOS NAND and NOR gates have been designed with $R_n = 1k\Omega$, $R_p = 2k\Omega$, $C_{out} = 8fF$, and $C_x = 2fF$, where C_x is the node capacitance between the series transistors.

- Calculate the worst-case rise and fall times for this NAND gate.
- Calculate the best-case rise time for this NAND gate.
- Calculate the worst-case rise time for a 2-input CMOS NOR gate.

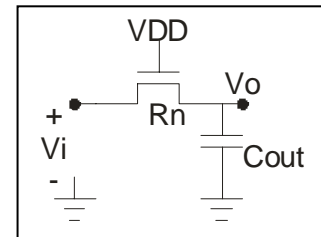
Problem 2

- Draw the schematic for the circuit that implements $F = x \cdot (y + z + w)$.
- Using an inverter with $\beta_n = \beta_p$, as a sizing reference, determine the size of each transistor in this circuit that will equalize the nMOS and pMOS resistances. That is, specify size of each transistor (in terms of β) relative to β_n or β_p .
- If, rather than scaling transistor sizes as in part (b), we leave them all at β_n or β_p , identify the signal path (through which transistors) that will produce the slowest response (rise and fall).

Problem 3

The circuit shown here describes an nMOS device used as a pass transistor. When the nMOS gate is high (VDD) it passes V_i to the output, which has a total capacitance of $C_{out} = 25fF$. Assuming $\beta_n = 0.5mA/V^2$, $V_{DD} = 3V$ and $V_{tn} = 0.5V$:

- What is the time constant associated with charging the output capacitance when $V_i = V_{DD}$?
- What is the *rise time* of this circuit?
- What is the *fall time* of this circuit when the input changes to $V_i = 0V$.

**Problem 4**

- Specify the parameters needed to determine the *activity coefficient* of a 2-input CMOS **NOR** gate. Calculate the activity coefficient.
- Calculate the dynamic power consumption of a 2-input CMOS **NOR** gate that drives a 12fF output capacitance at 100MHz from a 2V supply.
- If the quiescent (static) current in the NOR gate is 4nA, what percentage of the total power is due to dynamic power in the **NOR** gate?
- Specify the parameters needed to determine the activity coefficient of a 2-input CMOS **XOR** gate and calculate the activity coefficient.
- Using the parameters in b), calculate the dynamic power consumption of a 2-input CMOS **XOR** gate.

Problem 5

Draw the schematic for the following circuits and simulate to verify functionality in Cadence. Turn in the schematic and simulation results. All select and select_bar signals are available as inputs. Label the select inputs as s0, s1, etc. and the inverted signal as s0_bar, s1_bar, etc.

- 4:1 MUX using only transmission gates.
- 2/4 **active-low** decoder using transmission gates. Place a pull-up resistor at each output to ensure a high output for paths that are not selected.

Problem 6

- Draw the transistor-level schematic for a clocked latch using only tri-state circuits and an inverter (no transmission gates). You can use Cadence for the schematic but are not required to.
- Which transistors, if any, should be made larger if a large capacitive load must be driven? Label these on your schematic and discuss briefly why.