

**Problem 1**

2-input CMOS NAND and NOR gates have been designed with  $R_n = 1\text{k}\Omega$ ,  $R_p = 2\text{k}\Omega$ ,  $C_{out} = 8\text{fF}$ , and  $C_x = 2\text{fF}$ , where  $C_x$  is the node capacitance between the series transistors.

- Calculate the worst-case rise and fall times for this NAND gate.
- Calculate the best-case rise time for this NAND gate.
- Calculate the worst-case rise time for a 2-input CMOS NOR gate.

**Solution**

a) Worst case rise time is given by  $t_r = 2.2 R_p \cdot C_{out} = 2.2 * 2 \text{ K}\Omega * 8 \text{ fF} = 35.2 \text{ ps}$

The worst case fall time is given by  $t_f = 2.2 (2R_n \cdot C_{out} + R_n \cdot C_x)$   
 $= 2.2(2 * 1 \text{ K}\Omega * 8\text{fF} + 1\text{K}\Omega * 2\text{fF}) = 39.6\text{ps}$

b) The best-case rise time for a NAND gate occurs when both pMOS turn on and is given by  $t_r = 2.2 (R_p/2) \cdot C_{out}$ , where the total parallel resistance is  $R_p/2$ .  
 $= 2.2 * 2 \text{ K}\Omega/2 * 8 \text{ fF} = 17.6 \text{ ps}$

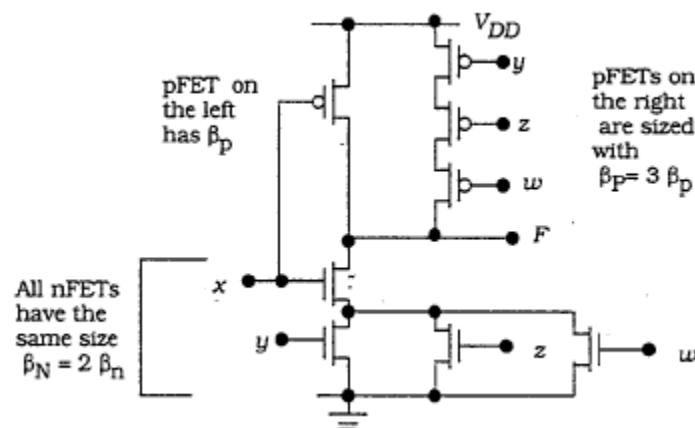
c) The worst-case rise time of a NOR gate is given by  $t_r = 2.2 (2R_p \cdot C_{out} + R_p \cdot C_x)$   
 $= 2.2(2 * 2 \text{ K}\Omega * 8\text{fF} + 2\text{K}\Omega * 2\text{fF}) = 79.2 \text{ ps}$

**Problem 2**

- Draw the schematic for the circuit that implements  $F = \overline{x \cdot (y + z + w)}$ .
- Using an inverter with  $\beta_n = \beta_p$ , as a sizing reference, determine the size of each transistor in this circuit that will equalize the nMOS and pMOS resistances. That is, specify size of each transistor (in terms of  $\beta$ ) relative to  $\beta_n$  or  $\beta_p$ .
- If, rather than scaling transistor sizes as in part (b), we leave them all at  $\beta_n$  or  $\beta_p$ , identify the signal path (through which transistors) that will produce the slowest response (rise and fall).

**Solution**

The circuit and relative device sizes are shown below



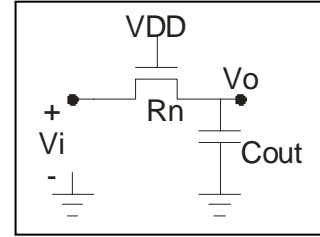
Worst case rise time: path through w, z, and y

Worst case fall time: path through x and only one of y, z, or w

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**Problem 3**

The circuit shown here describes an nMOS device used as a pass transistor. When the nMOS gate is high (VDD) it passes  $V_i$  to the output, which has a total capacitance of  $C_{out} = 25\text{fF}$ . Assuming  $\beta_n = 0.5\text{mA/V}^2$ ,  $V_{DD} = 3\text{V}$  and  $V_{tn} = 0.5\text{V}$ :



- What is the time constant associated with charging the output capacitance when  $V_i = V_{DD}$ ?
- What is the *rise time* of this circuit?
- What is the *fall time* of this circuit when the input changes to  $V_i = 0\text{V}$ .

**Solution:**

a) 
$$R_n = \frac{1}{\beta_n (V_{DD} - V_{th})} = \frac{1}{0.5\text{mA/V}^2 (3 - 0.5\text{V})} = 800\Omega$$

$$\tau_n = R_n \times C_{out} = 800\Omega \times 25\text{fF} = 20\text{ps}$$

b) 
$$t_r = 18\tau_n = 18(20\text{ps}) = 360\text{ps}$$

c) 
$$t_f = 2.94\tau_n = 2.94(20\text{ps}) = 58.8\text{ps}$$

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**Problem 4**

- Specify the parameters needed to determine the *activity coefficient* of a 2-input CMOS **NOR** gate. Calculate the activity coefficient.
- Calculate the dynamic power consumption of a 2-input CMOS **NOR** gate that drives a  $12\text{fF}$  output capacitance at  $100\text{MHz}$  from a  $2\text{V}$  supply.
- If the quiescent (static) current in the NOR gate is  $4\text{nA}$ , what percentage of the total power is due to dynamic power in the **NOR** gate?
- Specify the parameters needed to determine the activity coefficient of a 2-input CMOS **XOR** gate and calculate the activity coefficient.
- Using the parameters in b), calculate the dynamic power consumption of a 2-input CMOS **XOR** gate.

**Solution**

a) For the NOR gate, probability the output is at 0,  $p_0 = 0.75$

Probability the output is at 1,  $p_1 = 0.25$

The activity coefficient,  $a = p_0 \cdot p_1 = 0.75(0.25) = \underline{0.1875}$

b) 
$$P_{dyn} = a(C_{out})V_{DD}^2(f) = 0.1875 \cdot 12 \times 10^{-15} \cdot 2^2 \cdot 100 \times 10^6 = 900 \times 10^{-9} = \underline{0.9\mu\text{W}}$$

c) The static power is  $I_q \cdot V_{DD} = 4\text{n}(2) = 8\text{nW}$

So the total power =  $P_{dyn} + P_{static} = 900 + 8 = 908\text{nW}$

The percentage of total power that is dynamic power =  $900 / 908 = \underline{99.12\%}$

d) For the XOR gate,  $p_0 = 0.5$ ,  $p_1 = 0.5 \rightarrow a = p_0 \cdot p_1 = 0.5 \cdot 0.5 = \underline{0.25}$

e)  $P_{dyn} = \alpha(C_{out})V_{DD}^2(f) = 0.25 \cdot 12 \times 10^{-15} \cdot 2^2 \cdot 100 \times 10^6 = 1200 \times 10^{-9} = \underline{1.2 \mu W}$   
 So the XOR consumes 33% more power just due to activity coefficient. The variability of activity coefficients in CMOS logic gates makes it difficult to accurately model power consumption. Reliable estimates require analog simulations of the entire circuit over a random spread of input transitions.

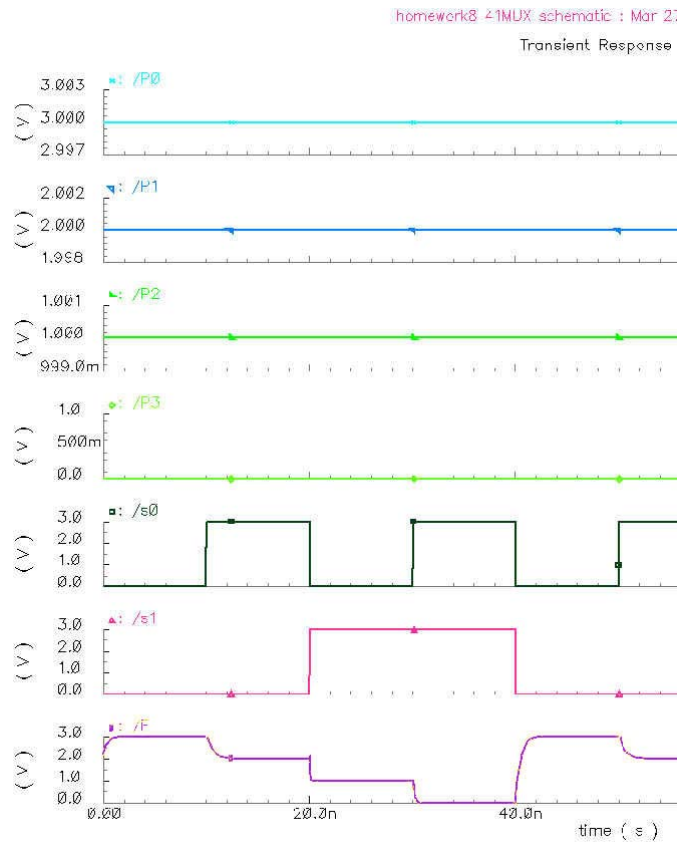
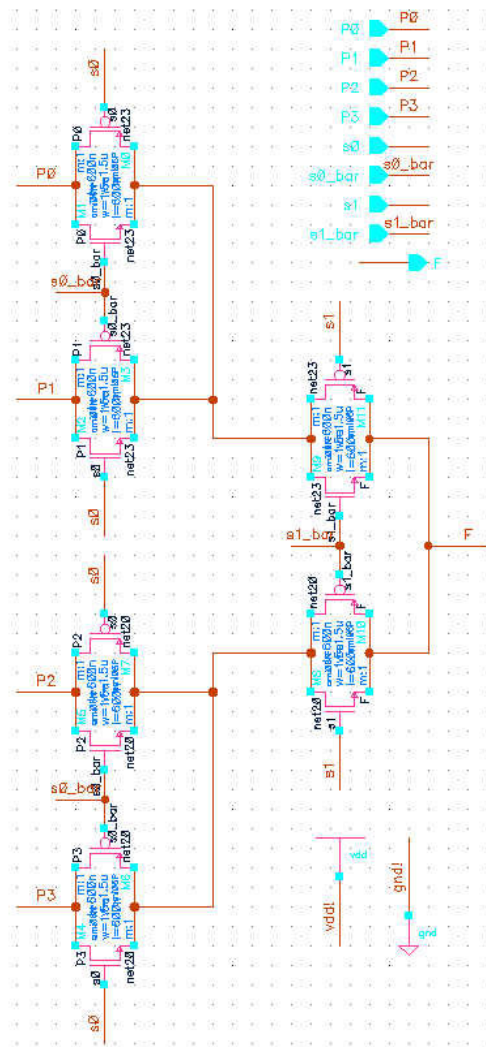
**Problem 5**

Draw the schematic for the following circuits and simulate to verify functionality in Cadence. Turn in the schematic and simulation results. All select and select\_bar signals are available as inputs. Label the select inputs as s0, s1, etc. and the inverted signal as s0\_bar, s1\_bar, etc.

- a) 4:1 MUX using only transmission gates.
- b) 2/4 active-low decoder using transmission gates. Place a pull-up resistor at each output to ensure a high output for paths that are not selected.

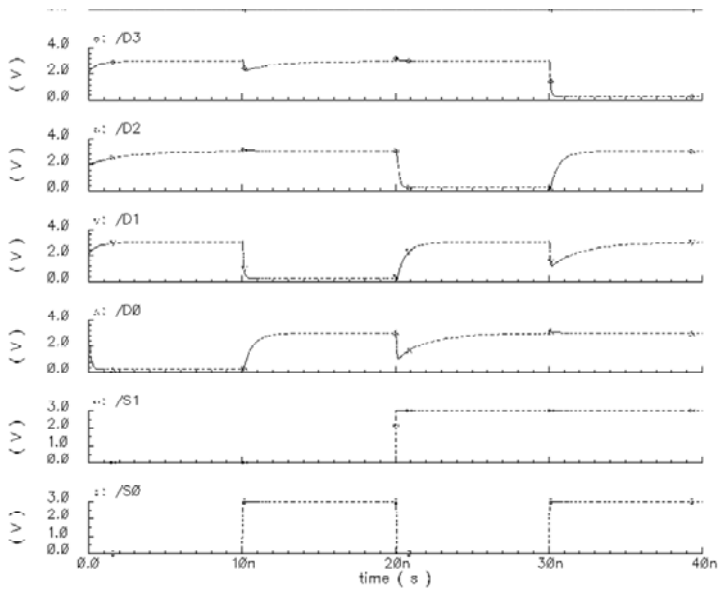
**Solution**

a) 4:1 MUX

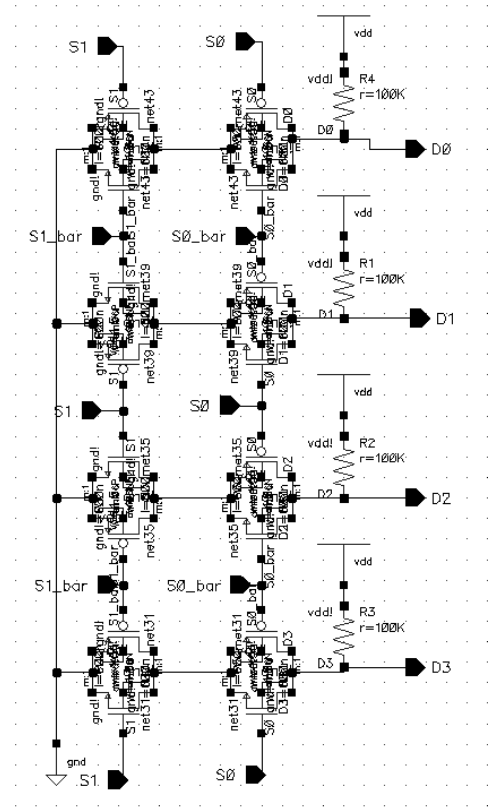


Here the inputs have been set to 0V, 1V, 2V and 3V to show the output is switching through these voltages as you change the selection inputs.

b) 2/4 active-low decoder



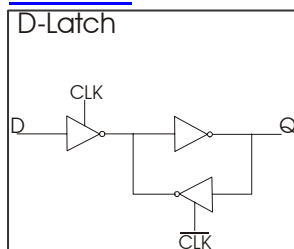
Notice the large undesirable spiking when two signals change simultaneously. This is an inherent problem with passgate circuit topologies. It also demonstrates an advantage of dynamic circuits, where data can be synchronized so that inputs change only while the output is precharging, thus eliminating erroneous output spikes during the evaluation stage.



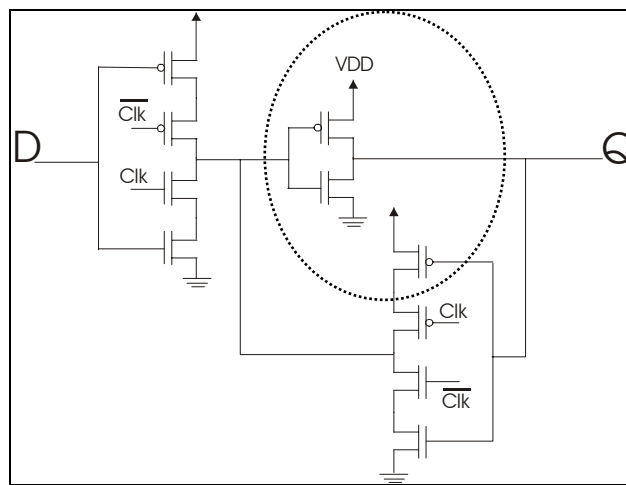
**Problem 6**

- Draw the transistor-level schematic for a clocked latch using only tri-state circuits and an inverter (no transmission gates). You can use Cadence for the schematic but are not required to.
- Which transistors, if any, should be made larger if a large capacitive load must be driven? Label these on your schematic and discuss briefly why.

**Solution**



(a)



(b)

Transistors circled in Figure (b) should be made larger because they drive the output.