

Problem 1

A NOR CMOS gate with the device/parasitic parameters below must drive (output to) the inputs of 3 NAND gates (one input on each gate) with the same MOSFET gate dimensions as the NOR gate.

$$\begin{aligned} V_{DD} &= 2.0V, C_{ox} = 2fF/\mu m^2, C_{DBp} = 1fF, C_{DBn} = 0.5fF \\ (W/L)_p &= 4/0.5, k'_p = 100\mu A/V^2, |V_{tp}| = 0.5V, \\ (W/L)_n &= 2/0.5, k'_n = 250\mu A/V^2, V_{tn} = 0.6V, \end{aligned}$$

- What is the total parasitic capacitance at the output of the NOR gate?
- What is the total load capacitance contributed by the 3 NAND gates?
- What is the total capacitance at the output of the NOR gate?
- What is the effective resistance between the output and VDD when the NOR gate pulls the output high? Use the “general” formula for channel resistance.
- Combining results from (c) and (d), what is the output RC time constant?

Problem 2

Assume the following process parameters and constants: $k'_n = 100 \mu A/V^2$, $k'_p = 40 \mu A/V^2$, $V_{tn} = |V_{tp}| = 0.5V$, $V_{SB} = 0V$ and $V_{DD} = 2.5V$. Ignore channel length modulation and other secondary effects.

- Use a computer (e.g., Excel, Matlab) to plot the I-V curve (I_D vs. V_D) for an nMOS transistor with $W=1.5\mu m$ and $L=0.6\mu m$, $V_S = 0V$ at $V_G = 1V$. Plot I_D vs. V_D from 0V to 2.5V with at least 10 steps. Be sure to properly account for transitions between the triode and saturation (active) regions.
- Repeat (a) at $V_G = 2V$ and $V_G = 2.5V$. Include all three curves on the same plot.
- Repeat (a) and (b) for a pMOS device with $W=3\mu m$, $L=0.6\mu m$ and $V_S = 2.5V$ and V_G values of 2V, 1V, and 0V. Notice that to plot I_D vs. V_D , you will need to be careful how you represent the term V_{SD} . Done correctly, your plot should be similar to the one shown in HW4 solutions.

Problem 3

For a CMOS inverter with the following parameters: $V_{DD} = 3V$, $V_{tn} = 0.6V$, $V_{tp} = -0.82V$, $k'_n = 100\mu A/V^2$, $\mu_n = 2.2\mu_p$:

- Determine the beta ratio, β_n/β_p , for a midpoint (switching threshold) of $V_M = 1.3V$.
- Determine the relative device widths, W_p/W_n , for $V_M = 1.3V$.

Problem 4

A CMOS inverter with minimum sized transistors has $\beta_n = 0.2mA/V^2$, $\beta_p = 0.1mA/V^2$ and $V_{tn} = |V_{tp}| = 0.6V$. Assume $V_{DD} = 3.3V$.

- What is the inverter gate switching threshold (midpoint) voltage V_M ?
- What is the resistance for each transistors using our general expression for MOSFET resistance in saturation?
- What are the rise and fall times of this circuit if the parasitic capacitance at the output is 9fF?
- If a load capacitance, $C_L = 25fF$ is added to the output, what are the new rise and fall times?
- What are the propagation delays for this circuit considering both parasitic and load capacitances?

Problem 5

A CMOS inverter is designed with $\beta_p = 80\mu\text{A}/\text{V}^2$, $\beta_n = 0.25\text{mA}/\text{V}^2$, $V_{tn} = |V_{tp}| = 0.5\text{V}$ and $V_{DD} = 2.5\text{V}$. The total capacitance at the output is 50fF

- a) Using our general expression for MOSFET resistance in saturation, what is the resistance for each transistor?
- b) What is the rise time of this circuit?
- c) What is the fall time of this circuit?
- d) What is the high-to-low propagation delay for this inverter?
- e) What is the low-to-high propagation delay for this inverter?
- f) Do the relative results (rise vs. fall time, high-to-low vs. low-to-high propagation delay) make sense considering the relative pMOS and nMOS beta values? Briefly explain why or why not.

Problem 6

A clever ECE410 student has noticed that the *simulated* worst-case rise time of a CMOS NAND gate is actually slower than the worst-case fall time, contrary to calculations based on the models give in class. The student proposes that a more accurate model of the NAND gate worst-case rise time should include an additional parameter.

- a) Specify the input transition sequence that would produce the worst-case rise time. Refer to your results from Lab 4 if necessary. Format your response like $AB \rightarrow CD$, where the first number represents the input to the series transistor that is connected to the output.
- b) Sketch an RC model of the NAND gate during this transition including all parasitic capacitances and resistances for all transistors that are turned on.
- c) Derive an improved equation for the worst-case rise time based on your RC model. You should see that an additional term is necessary to more accurately model this transition.
- d) Based on this improved model, will the worst-case rise time always be longer than the worst-case fall time? Briefly explain.