

**Problem 1**

A NOR CMOS gate with the device/parasitic parameters below must drive (output to) the inputs of 3 NAND gates (one input on each gate) with the same MOSFET gate dimensions as the NOR gate.

$$\begin{aligned} VDD &= 2.0V, C_{ox} = 2fF/\mu m^2, C_{DBp} = 1fF, C_{DBn} = 0.5fF \\ (W/L)_p &= 4/0.5, k'_p = 100\mu A/V^2, |V_{tp}| = 0.5V, \\ (W/L)_n &= 2/0.5, k'_n = 250\mu A/V^2, V_{tn} = 0.6V, \end{aligned}$$

- What is the total parasitic capacitance at the output of the NOR gate?
- What is the total load capacitance contributed by the 3 NAND gates?
- What is the total capacitance at the output of the NOR gate?
- What is the effective resistance between the output and VDD when the NOR gate pulls the output high? Use the "general" formula for channel resistance.
- Combining results from (c) and (d), what is the output RC time constant?

**solution**

a) A NOR gate has 1 pMOS and 2 NMOS drains at the output node.

Thus,  $C_{para} = C_{Dp} + 2C_{Dn}$

$$C_{Dp} = C_{GDp} + C_{DBp} \rightarrow \frac{1}{2} A_{Gp} C_{ox} + C_{DBp} = \frac{1}{2} (4 \cdot 0.5)(2) + 1 = 3 \text{ fF}$$

$$C_{Dn} = C_{GDn} + C_{DBn} \rightarrow \frac{1}{2} A_{Gn} C_{ox} + C_{DBn} = \frac{1}{2} (2 \cdot 0.5)(2) + 0.5 = 1.5 \text{ fF}$$

$$C_{para} = 3 + 2(1.5) = \underline{\underline{6 \text{ fF}}}$$

b) Each input of a NAND gate goes to 1 pMOS and 1 nMOS transistor. The capacitive load generated by gate (input) node of these transistors is just  $C_{Gp} + C_{Gn}$ .

$$\text{Thus, } C_L = 3 (C_{Gp} + C_{Gn}) = 3 C_{ox} (A_{Gp} + A_{Gn}) = 3 (2) (4 \cdot 0.5 + 2 \cdot 0.5)$$

$$\underline{\underline{C_L = 18 \text{ fF}}}$$

$$\text{c) } C_{out} = C_{para} + C_L = 6 + 18 = \underline{\underline{24 \text{ fF}}}$$

d) When the NOR gate pulls its output high, both series pMOS must be on.

Thus,  $R_{eff} = 2 R_p$ ,

$$R_p = [\beta_p (VDD - |V_{tp}|)]^{-1}, \beta_p = k'_p (W/L) = 100 (4/0.5) = 800 \mu A/V^2$$

$$R_p = [800 \mu (2.0 - |0.5|)]^{-1} = \underline{\underline{833 \Omega}}$$

$$\text{e) } \tau = R_p C_{out} = 833 (24 \text{ f}) = 20,000 \times 10^{-15} = 20 \times 10^{-12} = \underline{\underline{20 \text{ psec}}}$$

**Problem 2**

For the problems below assume the following process parameters and constants:  $k'_n = 100 \mu A/V^2$ ,  $k'_p = 40 \mu A/V^2$ ,  $V_{tn} = |V_{tp}| = 0.5V$ ,  $V_{SB} = 0V$  and  $VDD = 2.5V$ . Ignore channel length modulation and other secondary effects.

- Use a computer (e.g., Excel, Matlab) to plot the I-V curve ( $I_D$  vs.  $V_D$ ) for an nMOS transistor with  $W = 1.5 \mu m$  and  $L = 0.6 \mu m$ ,  $V_S = 0V$  at  $V_G = 1V$ . Plot  $I_D$  vs.  $V_D$  from  $0V$  to  $2.5V$  with at least 10 steps. Be sure to properly account for transitions between the triode and saturation (active) regions.
- Repeat (a) at  $V_G = 2V$  and  $V_G = 2.5V$ . Include all three curves on the same plot.

c) Repeat (a) and (b) for a pMOS device with  $W=3\mu\text{m}$ ,  $L=0.6\mu\text{m}$  and  $V_S = 2.5\text{V}$  and  $V_G$  values of 2V, 1V, and 0V. Notice that to plot  $I_D$  vs.  $V_D$ , you will need to be careful how you represent the term  $V_{SD}$ . Done correctly, your plot should be similar to the one shown in HW4 solutions.

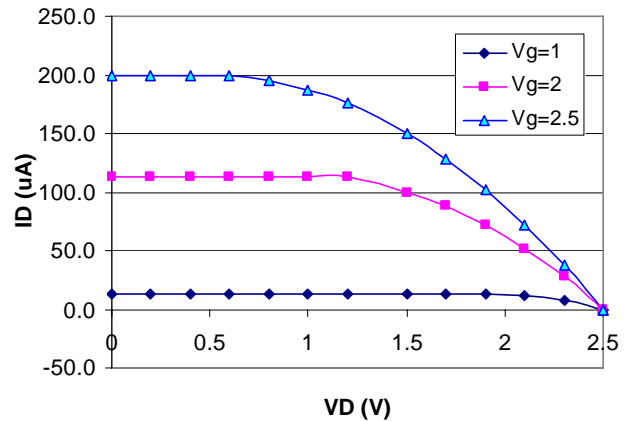
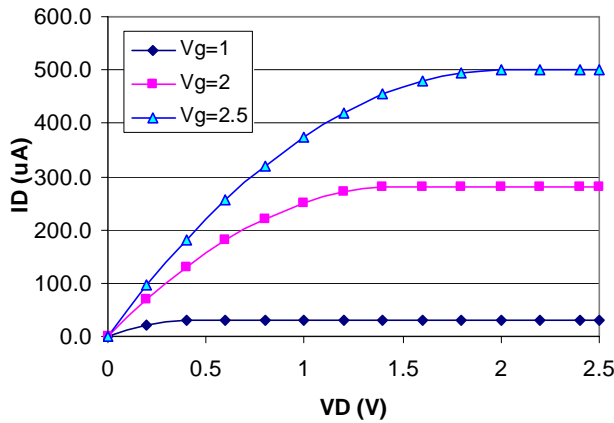
**Solution**

a & b)

Vds	Vg=1	Vg=2	Vg=2.5
0	0.0	0.0	0.0
0.2	20.0	70.0	95.0
0.4	30.0	130.0	180.0
0.6	31.3	180.0	255.0
0.8	31.3	220.0	320.0
1	31.3	250.0	375.0
1.2	31.3	270.0	420.0
1.4	31.3	280.0	455.0
1.6	31.3	281.3	480.0
1.8	31.3	281.3	495.0
2	31.3	281.3	500.0
2.2	31.3	281.3	500.0
2.4	31.3	281.3	500.0
2.5	31.3	281.3	500.0

c)

Vsd	Vds	Vg=1	Vg=2	Vg=2.5
2.5	0	12.5	112.5	200.0
2.3	0.2	12.5	112.5	200.0
2.1	0.4	12.5	112.5	200.0
1.9	0.6	12.5	112.5	199.5
1.7	0.8	12.5	112.5	195.5
1.5	1	12.5	112.5	187.5
1.3	1.2	12.5	112.5	175.5
1	1.5	12.5	100.0	150.0
0.8	1.7	12.5	88.0	128.0
0.6	1.9	12.5	72.0	102.0
0.4	2.1	12.0	52.0	72.0
0.2	2.3	8.0	28.0	38.0
0	2.5	0.0	0.0	0.0
0	2.5	0.0	0.0	0.0



**Problem 3**

This problem deals with a CMOS inverter with the following parameters:  $V_{DD} = 3\text{V}$ ,  $V_{tn} = 0.6\text{V}$ ,  $V_{tp} = -0.82\text{V}$ ,  $k'_n = 100\mu\text{A}/\text{V}^2$ ,  $\mu_n = 2.2\mu_p$ .

**Solution**

a) Determine the beta ratio,  $\beta_n/\beta_p$ , for a midpoint (switching threshold) of  $V_M = 1.3\text{V}$ .

$$\frac{\beta_n}{\beta_p} = \left( \frac{V_{DD} - V_M - |V_{Tp}|}{V_M - V_{Tn}} \right)^2 = \left( \frac{3 - 1.3 - 0.82}{1.3 - 0.6} \right)^2 = 1.58$$

b) Determine the relative device widths,  $W_p/W_n$ , for  $V_M = 1.3\text{V}$ .

$$\frac{\beta_n}{\beta_p} = \frac{k'_n(W/L)_n}{k'_p(W/L)_p} = 2.2 \frac{(W/L)_n}{(W/L)_p} = 1.58$$

The two aspect ratios are related by

$$(W/L)_p = 1.39(W/L)_n$$

---

**Problem 4**

A CMOS inverter with minimum sized transistors has  $\beta_n = 0.2\text{mA/V}^2$ ,  $\beta_p = 0.1\text{mA/V}^2$  and  $V_{tn} = |V_{tp}| = 0.6\text{V}$ . Assume  $V_{DD} = 3.3\text{V}$ .

- What is the inverter gate switching threshold (midpoint) voltage  $V_M$ ?
- What is the resistance for each transistors using our general expression for MOSFET resistance in saturation?
- What are the rise and fall times of this circuit if the parasitic capacitance at the output is  $9\text{fF}$ ?
- If a load capacitance,  $C_L = 25\text{fF}$  is added to the output, what are the new rise and fall times?
- What are the propagation delays for this circuit considering both parasitic and load capacitances?

**Solution**

$$\text{a) } V_M = \frac{V_{DD} - |V_{tp}| + V_{tn} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} = \frac{3.3 - 0.6 + 0.6\sqrt{2}}{1 + \sqrt{2}} = 1.47\text{V}$$

$$\text{b) } R_n = \frac{1}{\beta_n (V_{DD} - V_m)} = \frac{1}{(0.2)(2.7)} = 1.85\text{k}\Omega$$

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{tp}|)} = \frac{1}{(0.1)(2.7)} = 3.7\text{k}\Omega$$

$$\text{c) } t_{HL} = 2.2R_n C_{out} = 2.2(1.85\text{k}\Omega)(9\text{fF}) = 36.7\text{ps}$$

$$t_{LH} = 2.2R_p C_{out} = 2.2(3.7\text{k}\Omega)(9\text{fF}) = 73.3\text{ps}$$

**d) Here,  $C_{out} = 25 + 9 = 34\text{fF}$ , so**

$$t_{HL} = 2.2R_n C_{out} = 2.2(1.85\text{k}\Omega)(34\text{fF}) = 138.5\text{ps}$$

$$t_{LH} = 2.2R_p C_{out} = 2.2(3.7\text{k}\Omega)(34\text{fF}) = 277\text{ps}$$

$$\text{e) } t_{HL} = \ln(2)R_n C_{out} = \ln(2)(1.85\text{k}\Omega)(34\text{fF}) = 43.6\text{ps}$$

$$t_{LH} = \ln(2)R_p C_{out} = \ln(2)(3.7\text{k}\Omega)(34\text{fF}) = 87.3\text{ps}$$

---

**Problem 5**

A CMOS inverter is designed with  $\beta_p = 80\mu\text{A/V}^2$ ,  $\beta_n = 0.25\text{mA/V}^2$ ,  $V_{tn} = |V_{tp}| = 0.5\text{V}$  and  $V_{DD} = 2.5\text{V}$ . The total capacitance at the output is  $50\text{fF}$

- Using our general expression for MOSFET resistance in saturation, what is the resistance for each transistor?
- What is the rise time of this circuit?
- What is the fall time of this circuit?
- What is the high-to-low propagation delay for this inverter?
- What is the low-to-high propagation delay for this inverter?
- Do the relative results (rise vs. fall time, high-to-low vs. low-to-high propagation delay) make sense considering the relative pMOS and nMOS beta values? Briefly explain why or why not.

**Solution:**

$$\text{a) } R_n = \frac{1}{\beta_n (V_{DD} - V_m)} = \frac{1}{(0.25 \times 10^{-3})(2.5 - 0.5)} = 2.0\text{k}\Omega$$

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{tp}|)} = \frac{1}{(0.08 \times 10^{-3})(2.5 - 0.5)} = 6.25\text{k}\Omega$$

$$b) t_r = 2.2R_p C_{out} = 2.2(6.25k\Omega)(50 fF) = 685.5 ps$$

$$c) t_f = 2.2R_n C_{out} = 2.2(2k\Omega)(50 fF) = 220 ps$$

$$d) t_{HL} = \ln(2)R_n C_{out} = \ln(2)(2k\Omega)(50 fF) = 69.3 ps$$

$$e) t_{LH} = \ln(2)R_p C_{out} = \ln(2)(6.25k\Omega)(50 fF) = 217 ps$$

f) Because  $t_n > t_p$ , we should expect the fall time and high-to-low delay to be lower (faster) than the rise time and low-to-high delay. Calculation results confirm.

### Problem 6

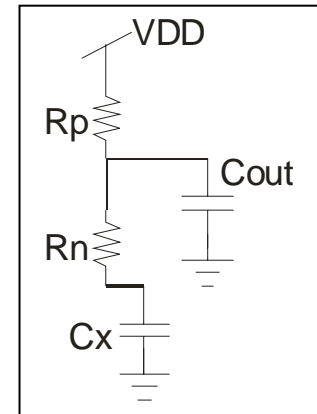
A clever ECE410 student has noticed that the *simulated* worst-case rise time of a CMOS NAND gate is actually slower than the worst-case fall time, contrary to calculations based on the models give in class. The student proposes that a more accurate model of the NAND gate worst-case rise time should include an additional parameter.

- Specify the input transition sequence that would produce the worst-case rise time. Refer to your results from Lab 4 if necessary. Format your response like AB → CD, where the first number represents the input to the series transistor that is connected to the output.
- Sketch an RC model of the NAND gate during this transition including all parasitic capacitances and resistances for all transistors that are turned on.
- Derive an improved equation for the worst-case rise time based on your RC model. You should see that an additional term is necessary to more accurately model this transition.
- Based on this improved mode, will the worst-case rise time always be longer than the worst-case fall time? Briefly explain.

### Solution

a) The worst-case rise time occurs when **11 → 10**, turning off the nMOS connected to ground but leaving the nMOS connected to the output turned on. Only one pMOS is turned on to pull the output high.

b) The RC model shown here includes the resistance of the nMOS transistor that remains on during the **11→10** transition and is connected to the output which is changed from low to high during this input transition.



c) For the RC circuit shown here there are two time constants,  $R_p C_{out}$ , and  $(R_p + R_n) C_x$ . The rise time is thus,

$$t_r = 2.2 (R_p \cdot C_{out} + (R_p + R_n) \cdot C_x)$$

d) No, it won't always be longer. The rise and fall times are given by

$$t_r = 2.2 (R_p \cdot C_{out} + (R_p + R_n) \cdot C_x)$$

$$t_f = 2.2 (2R_n \cdot C_{out} + R_n \cdot C_x)$$

Depending on the ratio  $C_{out}/C_x$  and the ratio  $R_p/R_n$ , the fall time could be longer than the rise time. For example, if  $R_p < 2R_n$  and  $C_{out} \gg C_x$  the fall time will be longer. Thus, the size of the transistors and the output load capacitance will determine which output transition is slowest. This is a feature of the NAND gate, which has very similar rise and fall characteristics, unlike the NOR gate where there is an obvious distinction and the fall time is always faster than the rise time.