ECE 410	Homework 5	Spring 2008

Problems 1-4 are on topics that will be covered on the exam 1 and may be good practice for the exam. Problem 5 will not be covered on exam 1. All of the problems must be completed and turned in for Homework 5. Note, Problem 1 is algebraically more difficult than what you might see on an exam, but concepts could be covered on the exam.

Problem 1
A pn junction is constructed by diffusing phosphorus (n-type) into a p-type silicon substrate doped at $N_A = 10^{15}$ cm^{-3}. The cross sectional area of the junction is 10µm^2.

a) Assuming a one-sided step junction is formed, calculate the minimum phosphorus doping concentration (N_D) that will ensure the junction capacitance is less than 1fF with no reverse bias.
b) If the calculated value of N_D is impractically high and must be reduced, will that increase or decrease the junction capacitance?
c) Will the junction capacitance increase or decrease if a reverse bias is applied?

Problem 2
A pMOS transistor has W/L=10 with process parameters $k'_p = 30\mu A/V^2$ and Vtp = -0.6V. For each of the cases below, identify the region of operation (cutoff, triode, saturation). Assume V_{SB} = 0V and VDD = 3V.

a) V_{SG} = 1V, V_{SD} = 3V
b) V_{SG} = 3V, V_{SD} = 2V
c) V_{SG} = 0.5, V_{SD} = 1V

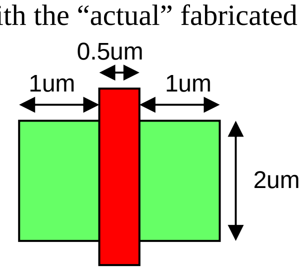
Problem 3
A pMOS transistor with a channel length modulation factor of $\lambda=0.05V^{-1}$ is sized so that it has a drain current of I_D=15µA when $V_{SD} = V_{SG}$-|Vtp|.

a) Accounting for channel length modulation what is the drain current if the drain voltage V_D drops by 2.5V? Note: you do have all the information needed.
b) Recognizing that the output resistance is defined as the change in drain voltage relative to the change in drain current, calculate the output resistance in the saturation (active) region.

Problem 4
A pMOS transistor of W=3µm and L=0.6µm has parameters tox = 500nm, surface mobility µp =200 cm^2 /V-sec and threshold voltage Vtp = -0.6V. VDD = 3V.

a) Calculate the transistor transconductance, βp.
b) Estimate the channel resistance, Rp, at V_{SG}=VDD.
c) If the lateral diffusion parameter is L_D=0.05µm, what is the effective channel length?
d) What is the percentage change in Rp using the effective channel length rather than the drawn length?

Problem 5
The simplified layout of a pMOS transistor in a 0.5µm process is shown here with the "actual" fabricated dimensions. Determine the device parasitics below using the following process model values:
$k'p = 90\mu A/V^2$, |Vtp| = 0.5V, Cox = 1.8fF/µm^2, Cj = 0.75fF/µm^2 and Cjsw = 0.25 fF/µm



a) What is the gate capacitance, C_G?
b) What is the gate-to-drain capacitance, C_{GD}?
c) What is the drain-to-bulk capacitance, C_{DB}?
d) What is the total capacitance at the drain node?
e) If the drain node RC time constant is 4psec, what is channel resistance?