

Problem 1

A pn junction is constructed by diffusing phosphorus (n-type) into a p-type silicon substrate doped at $N_A = 10^{15} \text{ cm}^{-3}$. The cross sectional area of the junction is $10 \mu\text{m}^2$.

- Assuming a one-sided step junction is formed, calculate the minimum phosphorus doping concentration (N_D) that will ensure the junction capacitance is less than 1fF with no reverse bias.
- If the calculated value of N_D is impractically high and must be reduced, will that increase or decrease the junction capacitance?
- Will the junction capacitance increase or decrease if a reverse bias is applied?

solution:

a) N_D must be greater than N_A because the n-type is diffused into the p-type. Because it's a one-sided step junction, $N_D \gg N_A$, and thus we can write the junction capacitance as

$$C_j = A \left[\frac{q\epsilon N_A}{2} \right]^{1/2} \left(\frac{1}{\sqrt{\Psi_0 + V_R}} \right)$$

Because $V_R = 0$, the only unknown is Ψ_0 , which is a function of the N_D we are looking for. To simply the algebra, let's define

$$C_{j0} = A \left[\frac{q\epsilon N_A}{2} \right]^{1/2}, \text{ thus } C_j = \frac{C_{j0}}{\sqrt{\Psi_0 + V_R}} = \frac{C_{j0}}{\sqrt{\Psi_0}}$$

Solving for Ψ_0 we get

$$\Psi_0 = \left(\frac{C_{j0}}{C_j} \right)^2 = V_T \ln \left(\frac{N_A N_D}{n_i^2} \right) \text{ and the only unknown is the } N_D \text{ we are looking for.}$$

Now we do the math...

$$C_{j0} = A \left[\frac{q\epsilon N_A}{2} \right]^{1/2} = 10 \times 10^{-8} \left[\frac{1.6 \times 10^{-19} \times 11.8 \times 8.85 \times 10^{-14} (10^{15})}{2} \right]^{1/2} = 9.14 \times 10^{-16}$$

$$\ln \left(\frac{N_A N_D}{n_i^2} \right) = \left(\frac{C_{j0}}{C_j} \right)^2 \Big/ V_T = \left(\frac{9.14 \times 10^{-16}}{1 \times 10^{-15}} \right)^2 \Big/ 0.025 = \frac{0.835}{0.025} = 33.4$$

$$\frac{N_A N_D}{n_i^2} = e^{33.4} = 3.2 \times 10^{14} \text{ and thus } N_D = \frac{3.2 \times 10^{14} \cdot n_i^2}{N_A} = 6.73 \times 10^{19}$$

which is possible, but impractically high since the concentration of silicon is only $\sim 10^{20}$.

b) decreasing N_D will decrease Ψ_0 and therefore increase junction capacitance

c) applying reverse bias will increase the depletion layer thickness, thus separating the charge and decreasing junction capacitance.

Problem 2

A pMOS transistor has $W/L=10$ with process parameters $k'_p = 30\mu\text{A}/\text{V}^2$ and $V_{tp} = -0.6\text{V}$. For each of the cases below, identify the region of operation (cutoff, triode, saturation). Assume $V_{SB} = 0\text{V}$ and $V_{DD} = 3\text{V}$.

- $V_{SG} = 1\text{V}$, $V_{SD} = 3\text{V}$
- $V_{SG} = 3\text{V}$, $V_{SD} = 2\text{V}$
- $V_{SG} = 0.5$, $V_{SD} = 1\text{V}$

solution:

The regions of operation for a pMOS transistor are defined as

Again, let's first define the regions

Cut Off	Saturation	Triode
$V_{SD} < V_{tp} $	$V_{SD} > V_{sat} = (V_{SG} - V_{tp})$	$V_{SD} < V_{sat} = (V_{SG} - V_{tp})$
$I_D = 0$	$I_D = \beta_p/2 (V_{SG} - V_{tp})^2$	$I_D = \beta_p/2 [2(V_{SG} - V_{tp}) V_{SD} - V_{SD}^2]$

Since W & L are constant, calculate $\beta_p = k'_p (W/L) = 30(10) = \underline{300\mu\text{A}/\text{V}^2}$

(a) $V_{SG} = 1\text{V}$, $V_{SD} = 3\text{V}$

$V_{sat} = (V_{SG} - |V_{tp}|) = 0.4\text{V}$; $V_{SD} > V_{sat} = (V_{SG} - |V_{tp}|)$; **saturation** region

$$I_D = \beta_p/2 (V_{SG} - |V_{tp}|)^2 = 150 (0.4)^2 = \underline{24\mu\text{A}}$$

(b) $V_{SG} = 3\text{V}$, $V_{SD} = 2\text{V}$

$V_{sat} = (V_{SG} - |V_{tp}|) = 2.4\text{V}$; $V_{SD} < V_{sat} = (V_{SG} - |V_{tp}|)$; **triode** region

$$I_D = \beta_p/2 [2(V_{SG} - |V_{tp}|) V_{SD} - V_{SD}^2] = 150 [2(2.4)(2) - (2)^2] = \underline{840\mu\text{A}}$$

(c) $V_{SG} = 0.5\text{V}$, $V_{SD} = 1\text{V}$

$V_{SG} < |V_{tp}|$ so the device is turned off; **cutoff** region

$$I_D = \underline{0\mu\text{A}}$$

Problem 3

A pMOS transistor with a channel length modulation factor of $\lambda=0.05\text{V}^{-1}$ is sized so that it has a drain current of $I_D=15\mu\text{A}$ when $V_{SD} = V_{SG}-|V_{tp}|$.

- Accounting for channel length modulation what is the drain current if the drain voltage V_D drops by 2.5V ? Note: you do have all the information needed.
- Recognizing that the output resistance is defined as the change in drain voltage relative to the change in drain current, calculate the output resistance in the saturation (active) region.

solution

a) At the onset of saturation, $I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_m)^2$. With channel length modulation,

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_m)^2 (1 + \lambda(V_{DS} - (V_{GS} - V_m)))$$

Thus, the ratio of currents for these two cases is just $1 + \lambda(V_{DS} - (V_{GS} - V_m)) =$

$1 + 0.05(2.5) = 1.125$, and the new $I_D = \underline{16.875\mu\text{A}}$.

$$\text{b) } r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{(15\mu\text{A} \cdot \lambda \cdot \Delta V_d)} = \frac{1}{15\mu\text{A} \cdot 0.05} = 1.333\text{M}\Omega$$

Problem 4

A pMOS transistor of $W=3\mu\text{m}$ and $L=0.6\mu\text{m}$ has parameters $t_{ox}=500\text{nm}$, surface mobility $\mu_p=200\text{ cm}^2/\text{V}\cdot\text{sec}$ and threshold voltage $V_{tp}=-0.6\text{V}$. $V_{DD}=3\text{V}$.

- Calculate the transistor transconductance, β_p .
- Estimate the channel resistance, R_p , at $V_{SG}=V_{DD}$.
- If the lateral diffusion parameter is $L_D=0.05\mu\text{m}$, what is the effective channel length?
- What is the percentage change in R_p using the effective channel length rather than the drawn length?

solution:

(a) The gate oxide capacitance per unit area is

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.6(8.85 \times 10^{-14})}{500 \times 10^{-7}} = 6.9\text{nF/cm}^2$$

The transistor transconductance is

$$\beta_p = \mu_p C_{ox} (W/L) = (200)(6.9\text{n})(3/0.6) = \underline{6.9\mu\text{A/V}^2}$$

(b) $R_p = 1 / (\beta_p (V_{DD} - |V_{tp}|)) = 1 / (6.9\mu (3 - 0.6)) = \underline{144/86\text{k}\Omega}$

(c) We don't have enough information to determine the depletion component, so we must assume it can be ignored. The effective channel length is therefore

$$L_{eff} = L - 2L_D = 0.6\mu\text{m} - 2(0.05\mu\text{m}) = \underline{0.5\mu\text{m}}$$

(d) Since R_p is linearly (and inversely) proportional to β and β is linearly (and inversely) proportional to L , we can setup a ratio to calculate the new 'effective' R_p .

$$\frac{R_p(eff)}{R_p} = \frac{\beta_p}{\beta_p(eff)} = \frac{L_{eff}}{L} \Rightarrow R_p(eff) = R_p \frac{L_{eff}}{L}$$

The percentage of change from R_p to $R_p(eff)$ can be expressed as

$$\%change = 100 \frac{R_p(eff) - R_p}{R_p} = 100 \frac{R_p \frac{L_{eff}}{L} - R_p}{R_p} = 100 \left(\frac{L_{eff}}{L} - 1 \right) = 100 \left(\frac{0.5}{0.6} - 1 \right) = \underline{-16.67\%}$$

where the negative sign reflects that the resistance has decreased.

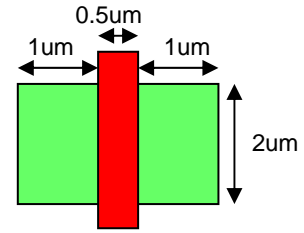
Problem 5

The simplified layout of a pMOS transistor in a 0.5 μm process is shown here with the “actual” fabricated dimensions. Determine the device parasitics below using the following process model values:

$$k'_p = 90\mu\text{A}/\text{V}^2, |V_{tp}| = 0.5\text{V}, C_{ox} = 1.8\text{fF}/\mu\text{m}^2, C_j = 0.75\text{fF}/\mu\text{m}^2$$

and $C_{jsw} = 0.25\text{fF}/\mu\text{m}$

- What is the gate capacitance, C_G ?
- What is the gate-to-drain capacitance, C_{GD} ?
- What is the drain-to-bulk capacitance, C_{DB} ?
- What is the total capacitance at the drain node?
- If the drain node RC time constant is 4psec, what is channel resistance?



solution:

a) $C_G = C_{ox} (W L) = (1.8\text{fF}/\mu\text{m}^2) (2\mu\text{m}) (0.5\mu\text{m}) = \boxed{1.8\text{fF}}$

b) $C_{GD} = \frac{1}{2} C_G = \frac{1}{2} (2\text{f}) = \boxed{0.9\text{fF}}$

c) $C_{DB} = C_j A_{Dbot} + C_{jsw} P_{DSW}$

$$A_{Dbot} = 2\mu\text{m} \times 1\mu\text{m} = 2\mu\text{m}^2$$

$$P_{DSW} = 2 (2\mu\text{m} + 1\mu\text{m}) = 6\mu\text{m}$$

$$C_{DB} = C_j A_{Dbot} + C_{jsw} P_{DSW} = 0.75\text{f} (2) + 0.25\text{f} (6) = \boxed{3\text{fF}}$$

d) Total capacitance at the drain node is

$$C_D = C_{GD} + C_{DB} = 0.9 + 3 = \boxed{3.9\text{fF}}$$

e) $\tau = R_n C_D \rightarrow R_n = \tau/C_D = 4\text{p}/3.9\text{f} = \boxed{1,025\ \Omega}$