

**REMINDER: You should always try to express answers in appropriate engineering-scale metric units. The common engineering units are factors of 3 ( $10^3$ ), such as mm,  $\mu\text{m}$ , nm or nF, pF, and fF. Unless otherwise noted in a problem, please convert scientific notation into the most appropriate engineering-scale metric units. This goes for all homework in ECE410.**

### Problem 1

Design a CMOS circuit to implement the following function.  $f = \overline{x \cdot (y \cdot z + z \cdot w)}$

- Construct the schematic for the circuit using the minimum number of transistors.
- Sketch the layout for this circuit using a stick diagram using colored pencils/pens/crayons. Show the Euler Path used for your stick diagram on your schematic. The stick diagram should include the active (green), poly (red), metal (blue), and contact (black X) layers and should be implemented between a power (VDD) and ground rail.

### Problem 2

Identify the fabrication process required to produce the following transistor/circuit features. Choose from the following options: photolithography, diffusion, ion implantation, dielectric deposition, thermal oxidation, chemical etching, or reactive ion etching.

- formation of a native oxide layer at high temperatures
- reproduction of a layout pattern onto a photoresist layer on the surface of a chip
- impurity doping with a maximum concentration at the surface of the wafer
- removal of material with an anisotropic profile
- creation of an insulator layer between metal layers

### Problem 3

A silicon p-n junction diode is doped with  $N_A = 10^{16} \text{ cm}^{-3}$  and  $N_D = 5 \times 10^{14} \text{ cm}^{-3}$ .

- Determine the built-in potential of this device
- Assuming  $\Psi_0 = 0.6\text{V}$  and no reverse bias, calculate the depletion width into the p-type region,  $x_p$  in  $\mu\text{m}$ .
- Assuming  $\Psi_0 = 0.6\text{V}$  and no reverse bias, calculate the depletion width into the n-type region,  $x_n$  in  $\mu\text{m}$ .
- Calculate the total depletion width as the sum of  $x_n$  and  $x_p$ .
- Calculate the total depletion width using the one-sided step junction approximation. What is the percentage error in this approximation?
- If  $N_D = 1 \times 10^{15} \text{ cm}^{-3}$ , would the error from the one-sided step junction approximation become larger or smaller?

### Problem 4

A  $2 \times 2 \mu\text{m}$  area of n+ is diffused into a p-type silicon substrate doped at  $N_A = 10^{16} \text{ cm}^{-3}$  to form a p-n junction diode that has a built-in potential of 0.75V.

- What is the donor concentration in the n+ region?
- Assuming  $N_D = 10^{17}$ , what is the total junction capacitance?
- If the equilibrium depletion width is  $0.5 \mu\text{m}$ , what is the depletion width if the n+ region is held at 3V relative to the p-type substrate? What is the junction capacitance at this bias voltage if the total junction capacitance at equilibrium is 1fF?

### Problem 5

- What is the oxide capacitance,  $C_{ox}$ , if the gate oxide of an nMOS transistor is 50nm thick?
- If  $C_{ox} = 30 \text{ nF/cm}^2$ ,  $W = 1.5 \mu\text{m}$  and  $L = 0.5 \mu\text{m}$ , what is the gate capacitance,  $C_g$ ?
- If  $C_g = 1\text{fF}$  and  $V_{tn} = 0.5\text{V}$  for the nMOS transistor, what is the value of the channel charge,  $Q_c$  when  $V_G = 1\text{V}$ ?

- d) For pMOS transistor, if  $C_g = 1\text{fF}$ ,  $V_{tp} = -0.5\text{V}$ , and  $V_{DD} = 2.5\text{V}$ , what is the value of the channel charge,  $Q_e$  when  $V_G = 1.5\text{V}$ ? This is not explicitly covered in class notes, so be careful with voltages and signs; think about what's going on physically.

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**Problem 6**

An nMOS transistor has  $W = 4.5\mu\text{m}$  and  $L = 0.6\mu\text{m}$  with process parameters  $k'_n = 110\mu\text{A}/\text{V}^2$  and  $V_{tn} = 0.6\text{V}$ . For each of the cases below, identify the region of operation (cutoff, triode, saturation) and calculate the drain current. Assume  $V_{SB} = 0\text{V}$  and  $V_{DD} = 2.2\text{V}$ .

- $V_{GS} = 2\text{V}$ ,  $V_{DS} = 1\text{V}$
- $V_{GS} = 2\text{V}$ ,  $V_{DS} = 2\text{V}$
- $V_{GS} = 0.5\text{V}$ ,  $V_{DS} = 2\text{V}$

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**Problem 7**

For each of the bias conditions below, clearly identify the region of operation (cutoff, triode, saturation) and calculate the drain current. Assume the following process parameters and constants:  $k'_n = 100\mu\text{A}/\text{V}^2$ ,  $k'_p = 40\mu\text{A}/\text{V}^2$ ,  $V_{tn} = |V_{tp}| = 0.5\text{V}$ ,  $V_{SB} = 0\text{V}$  and  $V_{DD} = 3\text{V}$ . Ignore channel length modulation and other secondary effects.

- an nMOS device with  $W = 1.5\mu\text{m}$  and  $L = 0.6\mu\text{m}$ ,  $V_S = 0\text{V}$ ,  $V_G = 2\text{V}$ ,  $V_D = 1\text{V}$
- an nMOS device with  $W = 1.5\mu\text{m}$  and  $L = 0.6\mu\text{m}$ ,  $V_S = 0\text{V}$ ,  $V_G = 1.5\text{V}$ ,  $V_D = 2.5\text{V}$
- a pMOS device with  $W = 3\mu\text{m}$  and  $L = 0.6\mu\text{m}$ ,  $V_S = V_{DD}$ ,  $V_G = 2.75\text{V}$ ,  $V_D = 0\text{V}$
- Use a computer (e.g., Excel, Matlab) to plot the I-V curve ( $I_D$  vs.  $V_D$ ) for a pMOS device with  $W = 3\mu\text{m}$ ,  $L = 0.6\mu\text{m}$ ,  $V_S = 3\text{V}$  and  $V_G = 2\text{V}$ . On the same plot, repeat for  $V_G = 1\text{V}$  and  $V_G = 0\text{V}$ . Be sure to properly account for transitions between the triode (ohmic) and saturation (active) regions.
- For the transistor in part (a), if  $V_{SB}$  increased to  $1\text{V}$  but all other parameters remained the same, would the current increase or decrease? Why (what effect is responsible)?