

Problem 1

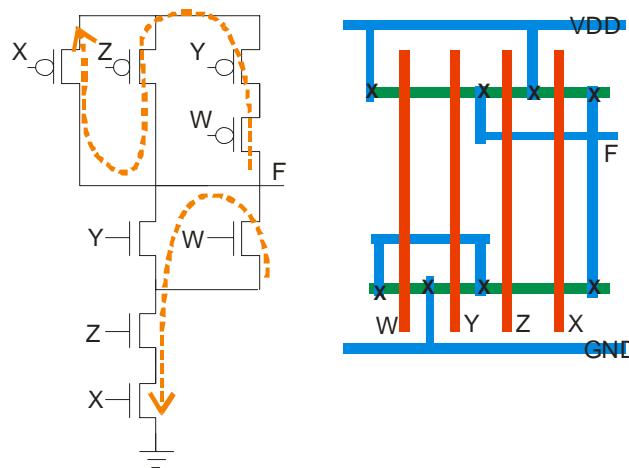
Design a CMOS circuit to implement the following function. $f = \overline{x \cdot (y \cdot z + z \cdot w)}$

- Construct the schematic for the circuit using the minimum number of transistors.
- Sketch the layout for this circuit using a stick diagram using colored pencils/pens/crayons. Show the Euler Path used for your stick diagram on your schematic. The stick diagram should include the active (green), poly (red), metal (blue), and contact (black X) layers and should be implemented between a power (VDD) and ground rail.

solution:

Reducing the function shows $f = \overline{x \cdot z \cdot (y + w)}$

The resulting schematic, with Euler Path, and stick diagram are below.



Notice the layout is organized so that only one continuous active region is needed for both the pMOS and the nMOS transistors. This is important for minimizing the space required for layout.

Problem 2

Identify the fabrication process required to produce the following transistor/circuit features.

Choose from the following options: photolithography, diffusion, ion implantation, dielectric deposition, thermal oxidation, chemical etching, or reactive ion etching.

solution:

- reproduction of a layout pattern onto a photoresist layer on the surface of a chip
photolithography
- impurity doping with a maximum concentration at the surface of the wafer
diffusion
- formation of a native oxide layer at high temperatures
thermal oxidation
- removal of material with an isotropic profile
chemical etching
- creation of an insulator layer between metal layers
dielectric deposition

Problem 3

A silicon p-n junction diode is doped with $N_A = 10^{16} \text{ cm}^{-3}$ and $N_D = 5 \times 10^{14} \text{ cm}^{-3}$.

- Determine the built-in potential of this device
- Assuming $\Psi_0 = 0.6 \text{ V}$ and no reverse bias, calculate the depletion width into the p-type region, x_p in μm .
- Assuming $\Psi_0 = 0.6 \text{ V}$ and no reverse bias, calculate the depletion width into the n-type region, x_n in μm .
- Calculate the total depletion width as the sum of x_n and x_p .
- Calculate the total depletion width using the one-sided step junction approximation. What is the percentage error in this approximation?
- If $N_D = 1 \times 10^{15} \text{ cm}^{-3}$, would the error from the one-sided step junction approximation become larger or smaller?

solution:

(a) The built-in potential is given by

$$\Psi_0 = V_T \ln \left(\frac{N_A N_D}{n_i^2} \right) = (0.026) \ln \left[\frac{(5 \times 10^{14})(10^{16})}{(1.45 \times 10^{10})^2} \right] = \boxed{0.621 \text{ V}}$$

(b) The depletion width into the n-type region is

$$x_p = \left[\frac{2\varepsilon(\Psi_0 + V_R)N_D}{qN_A(N_A + N_D)} \right]^{0.5} = \left[\frac{2(1.04 \times 10^{-12})(0.6)(5 \times 10^{14})}{1.6 \times 10^{-19}(10^{16})(1.05 \times 10^{16})} \right]^{0.5} = 6.09 \times 10^{-6} \text{ cm}$$

$$x_p = \mathbf{0.0609 \mu\text{m}}$$

(c) The depletion width into the p-type region is

$$x_n = x_p * N_A/N_D = 0.0609 * 10^{16}/5 \times 10^{14} = \mathbf{1.219 \mu\text{m}}$$

(d) The total depletion width is, $W = x_n + x_p = \mathbf{1.28 \mu\text{m}}$

$$(e) \quad W \cong \left[\frac{2\varepsilon(\Psi_0 + V_R)}{qN_A} \right]^{0.5} = \left[\frac{2(1.04 \times 10^{-12})(0.6)}{(1.6 \times 10^{-19})(5 \times 10^{14})} \right]^{0.5} = 1.249 \times 10^{-4} \text{ cm} \quad \mathbf{W = 1.249 \mu\text{m}}$$

The error from this estimate is % error = $100\% * |1.249 - 1.219| / 1.219 = \mathbf{2.42\%}$

f) If N_D were increased to 10^{15} cm^{-3} , the error would become larger since p-n junction will be less "one sided" and more of the depletion layer will spread into the n-side.

Problem 4

A $2 \times 2 \mu\text{m}$ area of n+ is diffused into a p-type silicon substrate doped at $N_A = 10^{16} \text{ cm}^{-3}$ to form a p-n junction diode that has a built-in potential of 0.75 V .

- What is the donor concentration in the n+ region?
- Assuming $N_D = 10^{17}$, what is the total junction capacitance?
- If the equilibrium depletion width is $0.5 \mu\text{m}$, what is the depletion width if the n+ region is held at 3 V relative to the p-type substrate? What is the junction capacitance at this bias voltage if the total junction capacitance at equilibrium is 1 fF ?

solution:

a) Solving the built-in potential equation for N_D we get

$$\Psi_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \Rightarrow N_D = \frac{n_i^2}{N_A} e^{(\Psi_0/V_T)} = \frac{(1.45 \times 10^{10})^2}{10^{16}} e^{(0.7/0.026)} \rightarrow N_D = \underline{7.085 \times 10^{16}}$$

b)

$$C_j = A \left[\frac{q \epsilon N_A N_D}{2(N_A + N_D)} \right]^{1/2} \left(\frac{1}{\sqrt{\Psi_0 + V_R}} \right) = 4 \times 10^{-8} \left[\frac{1.6 \times 10^{-19} \times 11.8 \times 8.85 \times 10^{-14} (10^{16})(10^{17})}{2(10^{16} + 10^{17})} \right]^{1/2} \frac{1}{\sqrt{0.75}}$$

$$C_j = 4 \times 10^{-8} (27.6 \times 10^9) (1.15) = 1.27 \times 10^{-15} = 1.27 \text{ fF}$$

c) Here we have a reverse bias of 3V. We can use the width equation to setup a ratio and quickly calculate the new biased width.

$$W = \left[\frac{2 \epsilon (\Psi_0 + V_R) N_D + N_A}{q N_D N_A} \right]^{1/2} \Rightarrow \frac{W_{new}}{W_{old}} = \frac{\sqrt{\Psi_0 + V_R}}{\Psi_0} \Rightarrow W_{new} = W_{old} \frac{\sqrt{\Psi_0 + V_R}}{\Psi_0}$$

$$W = 0.5 [(3+0.75)/0.75]^{1/2} = \underline{1.11 \mu\text{m}}$$

We can use the ratio approach to calculate the new depletion capacitance.

$$C_j = A \left[\frac{q \epsilon N_A N_D}{2(N_A + N_D)} \right]^{1/2} \left(\frac{1}{\sqrt{\Psi_0 + V_R}} \right) \Rightarrow \frac{C_{j,new}}{C_{j,old}} = \frac{\sqrt{\Psi_0}}{\sqrt{\Psi_0 + V_R}} \Rightarrow C_{j,new} = C_{j,old} \frac{\sqrt{\Psi_0}}{\sqrt{\Psi_0 + V_R}}$$

$$C_j = 1 [0.75/(3+0.75)]^{1/2} = \underline{0.447 \text{ fF}}$$

Problem 5

- What is the oxide capacitance, C_{ox} , if the gate oxide of an nMOS transistor is 50nm thick?
- If $C_{ox} = 30 \text{ nF/cm}^2$, $W=1.5 \mu\text{m}$ and $L=0.5 \mu\text{m}$, what is the gate capacitance, C_g ?
- If $C_g = 1 \text{ fF}$ and $V_{tn} = 0.5 \text{ V}$ for the nMOS transistor, what is the value of the channel charge, Q_c when $V_G=1 \text{ V}$?
- For pMOS transistor, if $C_g = 1 \text{ fF}$, $V_{tp} = -0.5 \text{ V}$, and $V_{DD}=2.5 \text{ V}$, what is the value of the channel charge, Q_c when $V_G=1.5 \text{ V}$? This is not explicitly covered in class notes, so be careful with voltages and signs; think about what's going on physically.

solution:

(a) $C_{ox} = \epsilon_{ox}/t_{ox} = (3.9)(8.85 \times 10^{-14}) / 50 \times 10^{-7} = 6.9 \times 10^{-8} \text{ [F/cm}^2\text{]}, \boxed{C_{ox} = 69 \text{ nF/cm}^2}$

(b) $C_g = C_{ox} W L = 3.0 \times 10^{-8} (1.5 \times 10^{-4}) (0.5 \times 10^{-4}) = 2.25 \times 10^{-16}, \boxed{C_g = 0.225 \text{ fF}}$

(c) $Q_c = - C_g (V_G - V_{tn}) = - 1 \times 10^{-15} (1 - 0.5) = -0.5 \times 10^{-15}, \boxed{Q_c = - 0.5 \times 10^{-15} \text{ Coulombs}}$

(d) $Q_c = C_g (V_{DD} - V_G - |V_{tp}|) = 1 \times 10^{-15} (2.5 - 1.5 - |-0.5|) = 0.5 \times 10^{-15}$

$\boxed{Q_c = 0.5 \times 10^{-15} \text{ Coulombs}}$

Notice that the charge is positive for pMOS and negative for nMOS. Make sure the reason for this is clear to you.

Problem 6

An nMOS transistor has $W=4.5\mu\text{m}$ and $L=0.6\mu\text{m}$ with process parameters $k'n = 110 \mu\text{A}/\text{V}^2$ and $V_{tn} = 0.6\text{V}$. For each of the cases below, identify the region of operation (cutoff, triode, saturation) and calculate the drain current. Assume $V_{SB} = 0\text{V}$ and $V_{DD} = 2.2\text{V}$.

- a) $V_{GS} = 2\text{V}$, $V_{DS} = 1\text{V}$
- b) $V_{GS} = 2\text{V}$, $V_{DS} = 2\text{V}$
- c) $V_{GS} = 0.5\text{V}$, $V_{DS} = 2\text{V}$

solution:

The regions of operation for an nMOS transistor are defined as

Cut Off	Saturation	Triode
$V_{GS} < V_{tn}$	$V_{DS} > V_{sat} = (V_{GS} - V_{tn})$	$V_{DS} < V_{sat} = (V_{GS} - V_{tn})$
$I_D = 0$	$I_D = \beta n/2 (V_{GS} - V_{tn})^2$	$I_D = \beta n/2 [2(V_{GS} - V_{tn}) V_{DS} - V_{DS}^2]$

(a) $V_{GS} = 2\text{V}$, $V_{DS} = 1\text{V}$

$V_{sat} = (V_{GS} - V_{tn}) = 1.4\text{V}$; $V_{DS} < V_{sat} = (V_{GS} - V_{tn})$; triode region

$$\beta n = k'n (W/L) = 825 \mu\text{A}/\text{V}^2$$

$$I_D = \beta n/2 [2(V_{GS} - V_{tn}) V_{DS} - V_{DS}^2] = 742.5 \mu\text{A}$$

(b) $V_{GS} = 2\text{V}$, $V_{DS} = 2\text{V}$

$V_{sat} = (V_{GS} - V_{tn}) = 1.4\text{V}$; $V_{DS} > V_{sat} = (V_{GS} - V_{tn})$; saturation region

$$I_D = \beta n/2 (V_{GS} - V_{tn})^2 = 808.5 \mu\text{A}$$

(c) $V_{GS} = 0.5\text{V}$, $V_{DS} = 2\text{V}$

$V_{GS} < V_{tn}$; cutoff region

$$I_D = 0\text{A}$$

Problem 7

For each of the bias conditions below, clearly identify the region of operation (cutoff, triode, saturation) and calculate the drain current. Assume the following process parameters and constants: $k'n = 100 \mu\text{A}/\text{V}^2$, $k'p = 40 \mu\text{A}/\text{V}^2$, $V_{tn}=|V_{tp}|=0.5\text{V}$, $V_{SB} = 0\text{V}$ and $V_{DD} = 3\text{V}$. Ignore channel length modulation and other secondary effects.

- a) an nMOS device with $W=1.5\mu\text{m}$ and $L=0.6\mu\text{m}$, $V_S = 0\text{V}$, $V_G = 2\text{V}$, $V_D = 1\text{V}$
- b) an nMOS device with $W=1.5\mu\text{m}$ and $L=0.6\mu\text{m}$, $V_S = 0\text{V}$, $V_G = 1.5\text{V}$, $V_D = 2.5\text{V}$
- c) a pMOS device with $W=3\mu\text{m}$ and $L=0.6\mu\text{m}$, $V_S = V_{DD}$, $V_G = 2.75\text{V}$, $V_D = 0\text{V}$
- d) Use a computer (e.g., Excel, Matlab) to plot the I-V curve (I_D vs. V_D) for a pMOS device with $W=3\mu\text{m}$, $L=0.6\mu\text{m}$, $V_S = 3\text{V}$ and $V_G = 2\text{V}$. On the same plot, repeat for $V_G = 1\text{V}$ and $V_G = 0\text{V}$. Be sure to properly account for transitions between the triode (ohmic) and saturation (active) regions.
- e) For the transistor in part (a), if V_{SB} increased to 1V but all other parameters remained the same, would the current increase or decrease? Why (what effect is responsible)?

solution:

The regions of operation for an nMOS transistor are defined above

(a) nMOS, $V_{GS} = 2\text{V}$, $V_{DS} = 1\text{V}$

$V_{sat} = (V_{GS} - V_{tn}) = 1.5\text{V}$; $V_{DS} < V_{sat} = (V_{GS} - V_{tn})$; triode region

$$\beta n = k'n (W/L) = 100 \mu (1.5/0.6) = 250 \mu\text{A}/\text{V}^2$$

$$I_D = \beta n/2 [2(V_{GS} - V_{tn}) V_{DS} - V_{DS}^2] = 250 \mu / 2 (2(1.5)1 - 1^2) = 250 \mu\text{A}$$

(b) $V_{GS} = 1.5V, V_{DS} = 2.5V$

$V_{sat} = (V_{GS} - V_{tn}) = 1V$; $V_{DS} > V_{sat} = (V_{GS} - V_{tn})$; **saturation** region

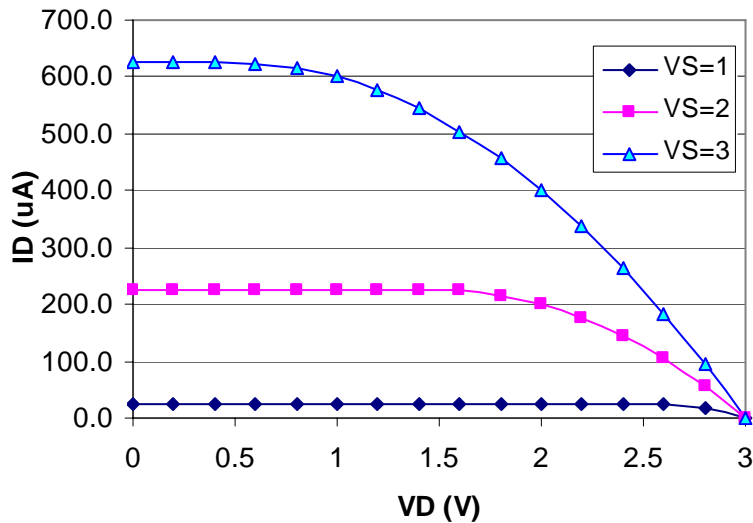
$$I_D = \beta_n/2 (V_{GS} - V_{tn})^2 = 250\mu/2 (1)^2 = \boxed{125\mu A}$$

(c) $V_{GS} = 3 - 2.75 = 0.25V, V_{DS} = 3V$

$V_{GS} < |V_{tp}|$; **cutoff** region

$$I_D = \boxed{0A}$$

(d)



(e) A non-zero source-to-bulk voltage would generate the body effect. If $V_{SB} > 0$, the threshold voltage for an nMOS device would increase. Higher V_{tn} would reduce current for the same V_{GS} .