

**Problem 1**

Draw the schematic for the CMOS circuit that implements the function  $F$  described by the truth table below. Use the least possible number of transistors. Explain your procedure and show the reduced function equation used to design the schematic.

Inputs			Output
X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

**solution (corrected)**

There are two basic approaches: we can construct a K-map or write a sum of products expression and reduce it. Let's try the sum of products option.

We can write the sum of products for either the high terms (F) or the low terms (F'). Because there are fewer low/zero terms, let's try those.

$$F' = (X'YZ' + X'YZ + XYZ') = X'Y(Z' + Z) + XYZ'$$

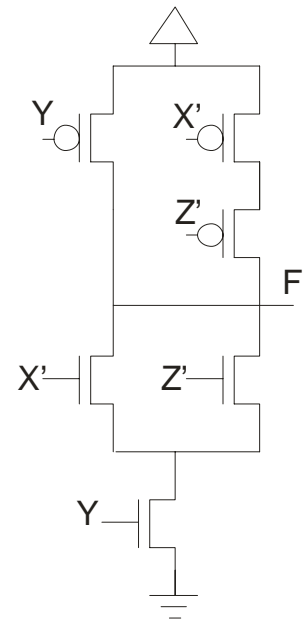
$$F' = X'Y + XYZ' = Y(X' + XZ') \rightarrow \underline{F' = Y(X' + Z')}$$

Thus  $\underline{F = Y' + XZ}$

Alternatively, by observation we can see that  $F = 1$  when  $Y'$  OR  $XYZ$  is true. Thus,  $F = Y' + XYZ$ . Using the property covered in HW1 we can reduce this to

$$\underline{F = Y' + XZ}$$

which matches our sum of products results. Note that we should get the same results if we started with the high terms sum of products.

**Problem 2**

Calculate the following for a sample of n-type silicon doped with  $N_d = 10^{15} \text{ cm}^{-3}$ . Assume  $\mu_n = 1500 \text{ cm}^2/\text{V}\cdot\text{sec}$  and  $\mu_p = 500 \text{ cm}^2/\text{V}\cdot\text{sec}$

- $n_n$  (free carrier electrons)
- $p_n$  (free carrier holes)
- conductivity of the sample
- resistance if the material is 1cm long, 100 $\mu\text{m}$  wide, and 1 $\mu\text{m}$  thick.

**solution:**

a)  $n_n \approx N_d = 10^{15} \text{ cm}^{-3}$

b)  $p_n = n_i^2/n_n = (1.45 \times 10^{10})^2 / 10^{15} = 2.10 \times 10^5 \text{ cm}^{-3}$

c) The conductivity of n-type material is given by

$$\sigma = q(\mu_n n_n + \mu_p p_n) = (1.60 \times 10^{-19})[(1500)(10^{15}) + (500)(2.10 \times 10^5)] = 0.24 \text{ } (\Omega\text{-cm})^{-1}$$

d) The resistance of the material is

$$R = \frac{L}{\sigma A} = \frac{1}{(0.24)(100 \times 10^{-4})(1 \times 10^{-4})} = 4.17 \text{ M}\Omega$$

### Problem 3

A pMOS transistor has  $W = 1.5\mu\text{m}$  and  $L = 0.5\mu\text{m}$ . What is the oxide thickness of the gate capacitance,  $C_G$ , is 1fF? Express your answer in angstroms.

### solution

$$C_G = W L C_{ox} \rightarrow C_{ox} = C_G / (WL) = 1 / (1.5 \times 0.5) \times 10^{-3} = 1.33 \times 10^{-3} \text{ [F/m}^2\text{]}$$

Before we continue, let's express this in centimeters:

$$C_{ox} = 1.33 \times 10^{-3} (1/100)^2 = 1.33 \times 10^{-7} \text{ [F/cm}^2\text{]}$$

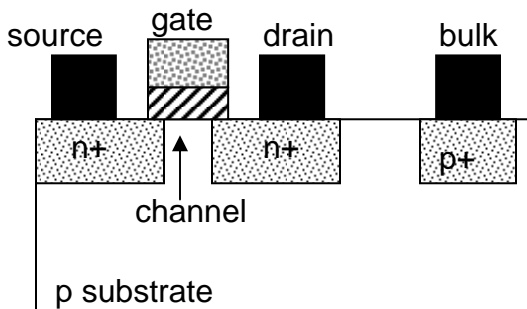
$$\text{Now, } C_{ox} = \epsilon_{ox} / t_{ox} \rightarrow t_{ox} = \epsilon_{ox} / C_{ox} = (3.9 \times 8.85 \times 10^{-14}) / 1.33 \times 10^{-7} \text{ [cm]}$$

$$t_{ox} = 25.95 \times 10^{-7} \text{ cm} = 25.95 \times 10^{-9} \text{ meters} = \underline{259.5 \text{ \AA}}$$

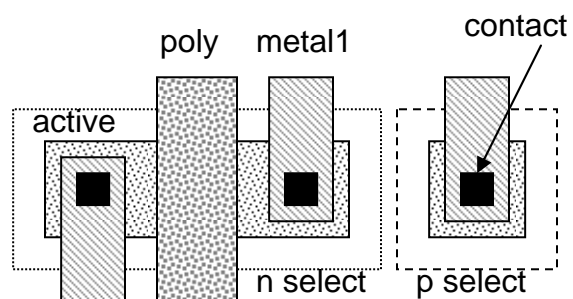
### Problem 4

- Draw the cross-section (profile) of a 4-terminal nMOS transistor and label all important regions of the device.
- Draw the top view of a 4-terminal nMOS transistor showing all of the layout layers and features necessary to construct a complete *four-terminal* device.
- Repeat steps a) and b) for a pMOS transistor.
- Which step in the LOCOS process defines the channel width (W) of a MOSFET?

### solution

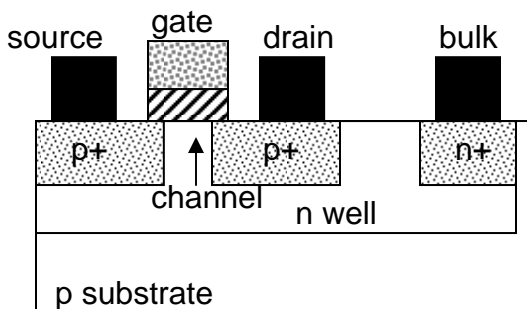


nMOS profile

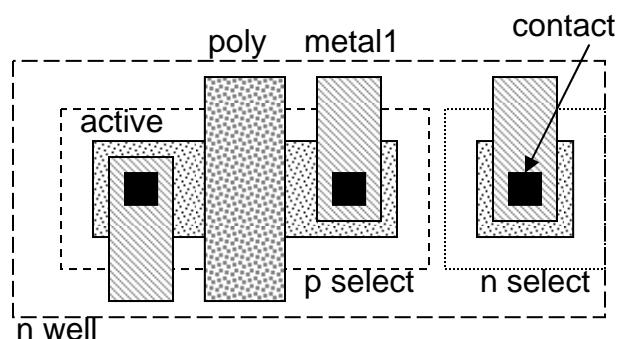


nMOS layout top view

a) and b)



pMOS profile



pMOS layout top view

c)

d) The width of a MOSFET is set by the size of the **ACTIVE** layer.

### Problem 5

List the SCMOS design rule (minimum size/dimension) in units of lambda ( $\lambda$ ) for the following layout features. You will have to visit the MOSIS design rules website, linked on the class/lab webpage.

#### solution

a) spacing between n-wells at same potential

$$6\lambda$$

b) spacing between actives of different implant (doping type)

$$4\lambda$$

c) poly spacing to active (outside of a transistor)

$$1\lambda$$

d) active overlap of contact

$$1.5\lambda$$

e) contact size

$$2\lambda$$

f) metal-1 spacing

$$2\lambda$$

### Problem 6

Sketch a color-coded stick diagram for the circuit that implements the function  $f = \overline{a + b \cdot c + d}$ .

Organize the layout so that the transistors can be implemented on a continuous strip of active (i.e., do not break the active).

#### solution:

An interesting feature of this function is that you have to organize the transistors within the schematic correctly in order to achieve the 'one continuous strip of active' layout goals. The schematic below shows one possible implementation. Notice the b || c pMOS devices must be directly attached to either the ground or output nodes in order to draw a loop that does not violate the rules. Two possible loops (with X at the start and an arrow at the end) for this schematic implementation are shown (solid-orange line and dotted-blue line). The solid-orange loop is used to set the order of poly traces in the stick diagram below to a, d, b, c. However, there are many possible layouts for this function.

