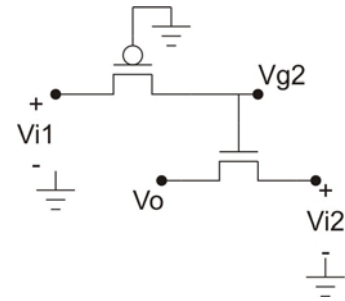


Problem 1

Using the rules given in lecture notes, find V_{g2} and V_o required for both transistors to be ON in the two-transistor circuit shown below for each of the listed input voltage combinations. Assume $V_{DD} = 2.5V$, $V_{tn} = 0.5V$, and $|V_{tp}| = 0.5V$.



- (a) $V_{i1} = 0V$, $V_{i2} = 0V$
- (b) $V_{i1} = 2V$, $V_{i2} = 2V$
- (c) $V_{i1} = 2.5V$, $V_{i2} = 2.5V$
- (d) $V_{i1} = 0V$, $V_{i2} = 1V$

Problem 2

Design a transistor-level CMOS logic circuit to implement the function $F = \overline{(x + yz)} \cdot (w + x)$ using the least number of transistors.

HINT: Consider that you may need to expand the equation in order to reduce it using the logic properties shown in the Chapter 2 lecture notes.

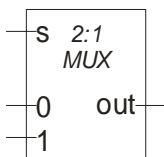
Problem 3

Construct the CMOS logic circuit that implements $Y = a + \overline{a} + b + c\overline{b}$ using the fewest possible transistors. You are allowed to use inverted inputs (e.g., \overline{a}) rather than adding inverters to create these signals.

Problem 4

The symbol for a 2:1 multiplexer and the truth table for a 4:1 multiplexer are shown below.

- a) Construct a schematic for a 2:1 MUX using two CMOS transmission gates and an inverter.
- b) Using the 2:1 MUX symbol below, construct a gate-level schematic for a 4:1 multiplexer using only 2:1 multiplexers. The inputs should be s_0 , s_1 , and $P_{3:0}$ ($P_0 - P_3$) and the output is F .
- c) How many transistors are needed to form the transmission gate based 4:1 MUX in (b)?
- d) Are there any redundant transistors that could be eliminated if you constructed the 4:1 MUX at the transistor level? If so, how many and which ones?



s_1	s_0	F
0	0	P_0
0	1	P_1
1	0	P_2
1	1	P_3

<more on next page>

Problem 5

A CMOS metal layer with resistivity, ρ , $3 \times 10^{-6} \Omega\text{-cm}$ is $0.6\mu\text{m}$ thick. It is used to draw a signal trace that is $100\mu\text{m}$ long and $0.75\mu\text{m}$ wide.

- a) Calculate the sheet resistance, R_s , of this metal layer.
- b) How many "squares", n , are in the signal trace?
- c) Use the results in (a) and (b) to determine the resistance of the trace.

Problem 6

A polysilicon trace that is $0.6\mu\text{m}$ wide, 0.05mm long, and $0.5\mu\text{m}$ thick has a sheet resistance of 20Ω . It is used to form a high frequency signal trace.

- a) Calculate the resistance of the poly trace.
- b) Calculate the line capacitance of this signal trace assuming the line is separated from a conducting plate by a 100\AA thick oxide layer. Express your answer in fF (10^{-15})
- c) Calculate the time constant (RC-delay) associated with this trace.