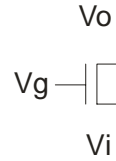


Problem 1

For problems 2-4 below, find the voltages required to keep the transistor 'on' by applying the rules discussed in class. Assume $V_{DD} = 2.2V$

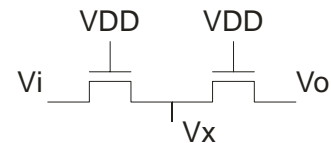


	FET type	$ V_t $ (V)	V_g (V)	V_i (V)
a	n-type	0.5	2.2	1
b	n-type	0.6	1.5	1
c	p-type	0.4	0	2
d	p-type	0.5	1.7	2
e	p-type	0.5	1	1.5

Problem 2

Find the midpoint voltage, V_x , and output voltage, V_o , for the chain of two nFET pass transistors shown below for the following cases. Assume $V_{DD} = 2.5V$ and $V_{tn} = 0.5V$.

- (a) $V_i = 0V$
 (b) $V_i = 1.1V$
 (c) $V_i = 2.2V$

**Problem 3**

Using fundamental logic properties, prove the following logic relationships

- (a) $(a+b)(a+c) = a+bc$
 (b) $a + a'b = a + b$

Problem 4

Design a CMOS logic gate for the function $f = \overline{x + y \cdot (z + x)}$ using the least number of transistors by completing the following steps:

- Identify the nMOS portion of the circuit by setting up and reducing the equation for f_n and then implementing this equation as a **gate-level** schematic. Note, because this is nMOS logic, the gate-level schematic should have an inversion at the output but no inversions at the inputs (assert-high logic).
- Apply bubble pushing on the **gate-level** schematic in (a) to construct the gate-level schematic for the pMOS portion of the circuit. Here, the bubble at the output must be pushed to the inputs and all inputs must have a bubble on them (assert-low logic). Be sure to properly apply the DeMorgan relations and modify logic gates appropriately.
- Use the gate-level schematic in (a) to construct the **transistor-level** schematic for the nMOS portion of the circuit, properly applying the series/parallel transistor rules for each AND and OR function.
- Repeat part (c) for the pMOS portion of the circuit, adding this to the top of the nMOS portion to form a complete CMOS logic circuit.

Problem 5

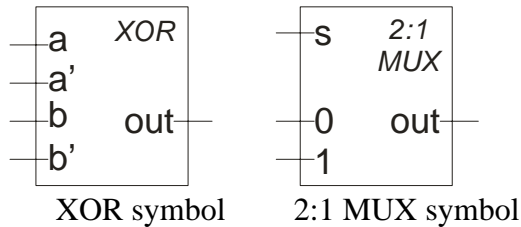
Follow the procedure below to construct the CMOS logic gate for the function $f = \overline{\overline{a + b \cdot c}}$.

- a) Write the equation for the nMOS network.
- b) Write the equation for the pMOS network.
- c) Use the equations in (a) and (b) to construct a schematic for f .
- d) Verify the nMOS and pMOS networks are proper complements (series groups in nMOS are parallel in pMOS, etc.).

Problem 6 (Design Challenge)

a) As discussed in lecture, the XOR and XNOR CMOS schematics are very similar; they have exactly the same structure but two of the inputs are different. Based on this, construct a **gate-level** schematic (no transistors, just gate symbols) for a circuit that uses only one XOR gate to implement both XOR and XNOR functions. The symbol for the CMOS XOR gate is shown below, having inputs **a**, **a'** (NOT a), **b**, and **b'** (NOT b). A signal **S** should be used to select between the XOR and XNOR function. You can use any additional INV, MUX, NAND and NOR gates needed to implement this function. The completed gate should only have inputs **M**, **N**, and **S** and output **Z** such that:

- if $S = 0$, $Z = M \text{ XOR } N$
- if $S = 1$, $Z = M \text{ XNOR } N$



Notice that you will have to use inverters to eliminate the need for inverted inputs (N' or M').

- b) Assuming the 2:1 MUX has a built-in control signal inverter and requires 6 transistors, how many transistors does your design require?