

NAME: _____

Exam 1

ECE 410 Fall 2002

During this exam you are allowed to use a calculator and the equations sheet provided. You are not allowed to speak to or exchange books, papers, calculators, etc. with other students.

Total Points: 100

Time: 60 minutes (11:30pm – 12:30pm)

- Write your name at the top of the exam and your initials at the top of each sheet.
- **Sign the honor pledge at the end of the exam.**
- Show all of your work. Try to use only the pages provided (write on back if necessary)
- Give units in your answers.
- Note the point value of each question and try to at least attempt each problem. Partial credit will be given for all problems involving calculations.

True or False: For each of the following statements, circle T if it is true and F if it is false.

2 pts. each.

- T F 1. Two *series* switches controlled by A and B form the function A OR B.
- T F 2. The maximum output voltage from a pMOS transistor with its Source connected to VDD will be $VDD - |V_{tp}|$.
- T F 3. In a CMOS inverter, when the input is logic-high, the pMOS device is ON and the nMOS device is OFF.
- T F 4. A CMOS NAND gate contains two parallel pMOS transistors.
- T F 5. In a CMOS gate, if the inputs to nMOS are A and B, the inputs to pMOS will be A' and B'.
- T F 6. A transmission gate is formed by placing an nMOS transistor in series with a pMOS transistor and connecting both inputs to a select/control signal.
- T F 7. In the fabrication process of diffusion, the dopant concentration is greatest at the exposed (top) surface of the substrate wafer.
- T F 8. Adding multiple contacts between layout layers (e.g., metal and poly) increases the resistance.
- T F 9. The width of a pn junction depletion layer depends highly on the dopant concentration in the lightly doped side of the junction.
- T F 10. Propagation delay describes the time it takes for the input to rise from a low value to a high value.

Multiple Choice: In the box beside each question, write the letter for the ONE answer that best fits the question/statement. 3 pts. each.

11. Which of the following is a reason why silicon CMOS circuits dominates the IC industry?
 A) can get more CMOS gates in same chip area B) CMOS gates are faster than any other logic structures
 C) silicon is an expensive material D) CMOS physics is complex to understand
12. Which of the following is a layout layer in an n-well CMOS process?
 A) n-type substrate B) contact
 C) p-well D) transistor gate
13. Which of the following CMOS logic circuits will contain parallel nMOS transistors?
 A) NOR B) Transmission Gate
 C) NAND D) Inverter
14. Which of the following CMOS gates can be implemented using AOI structured logic?
 A) Inverter B) XOR
 C) Transmission Gate D) none of the above
15. Which of the following would have the highest mobility, μ .
 A) electrons deep in the substrate B) electrons near the surface of the substrate
 C) holes deep in the substrate D) holes near the surface of the substrate
16. Which of the following layers is NOT needed to layout an nMOS transistor?
 A) active B) via
 C) poly D) n-select
17. A nMOS transistor will have a collection of positive charges under the gate oxide during:
 A) accumulation B) depletion
 C) inversion D) all of the above
18. Which of the following circuits would utilize an nMOS shared junction without contact?
 A) INV B) NOR
 C) NAND D) NOR3
19. Which of the following is a disadvantage of using high-level metals within primitive cells?
 A) higher transistor packing density B) more metal layers needed for complete chip layout
 C) less chip area required for routing D) less resistance between cells
20. Which of the following causes the drain current to increase with V_{DS} in the saturation region?
 A) channel length modulation B) inversion charge in the channel
 C) the body effect D) hole mobility

Calculation: Solve the following problems in the space provided and on the backs of these pages if necessary. You must show ALL major step on these test pages. Unless otherwise noted, for all problems assume minimum feature size = $2\lambda = 0.6\mu\text{m}$, and $V_{DD} = 3V$.

21. Conductivity & RC Model: [15 points]

Consider the nMOS transistor shown to the right which has a substrate doping of $N_A = 1 \times 10^{16} \text{cm}^{-3}$.

- a) What is the electron concentration in the channel at equilibrium (no bias voltages)?

ANSWER: $n_p = \underline{\hspace{2cm}} \text{cm}^{-3}$

- b) What is the hole concentration in the channel at equilibrium?

ANSWER: $p_p = \underline{\hspace{2cm}} \text{cm}^{-3}$

- c) If the equilibrium channel conductivity is $0.04 [\Omega\text{-cm}]^{-1}$ what is the equilibrium resistance of the channel (from source to drain)? Include lateral diffusion under the gate in your calculation.

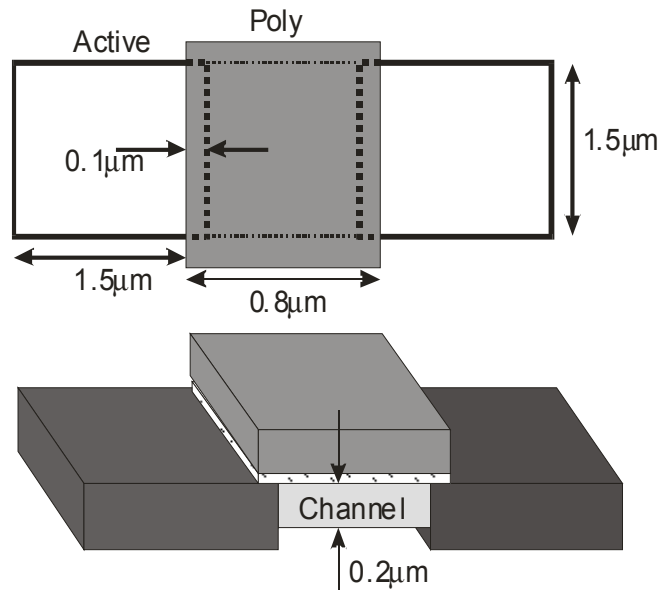
ANSWER: $R = \underline{\hspace{2cm}} [\text{k}\Omega]$

- d) What is the drain capacitance of this device under zero-bias pn junction conditions assuming $C_{ox} = 3\text{fF}/\mu\text{m}^2$, $C_j = 1\text{fF}/\mu\text{m}^2$, and $C_{jsw} = 0.2\text{fF}/\mu\text{m}$? Include effects of lateral diffusion.

ANSWER: $C_D = \underline{\hspace{2cm}} [\text{fF}]$

- e) What is the RC time constant, τ_n , of this device at the drain node if the source is connected to ground and the resistance of the channel during inversion is $R_n = 100\Omega$? Assume $C_D = C_S = 20\text{fF}$.

ANSWER: $\tau_n = \underline{\hspace{2cm}} [\text{psec}]$



22. MOSFET Voltages: 10 points

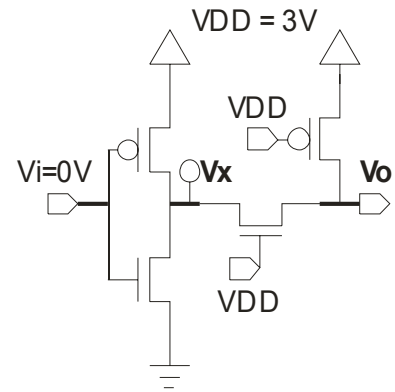
Find the requested voltages in the following circuit by applying the rules for cases where 2 terminal voltages are known. Assume $V_{tn} = |V_{tp}| = 0.5V$ for all transistors.

a) For the circuit on the right, what is the voltage at the output of the inverter, V_x ?

ANSWER: $V_x =$ _____ V

b) What is V_o ?

ANSWER: $V_o =$ _____ V



23. MOSFET Currents: 13 points

a) For each of the following bias voltages, specify the region of operation (cutoff, triode, or saturation). Assume $V_{tn} = |V_{tp}| = 0.5V$.

i) nMOS with $V_D = 2V$, $V_G = 1V$, and $V_S = 0V$.

REGION: _____

ii) nMOS with $V_D = 2V$, $V_G = 0V$, and $V_S = 1V$.

REGION: _____

iii) pMOS with $V_D = 2V$, $V_G = 1V$, and $V_S = 3V$.

REGION: _____

iv) pMOS with $V_D = 0V$, $V_G = 1.5V$, and $V_S = 3V$.

REGION: _____

b) For case (i) above, calculate the nMOS drain current neglecting body effect and channel length modulation and do not adjust for effective channel length.

Assume $W=1.8\mu m$, $L=0.6\mu m$ and $\mu C_{ox} = 50\mu A/V$.

ANSWER: $I_D =$ _____ μA

23. CMOS Logic: 12 points

a) Reduce the following function to a form that can be implemented in CMOS with the fewest number of transistors. Show all steps, and give the final equation for the nMOS block, $F_n = F'$.

$$F = \overline{A + B + \overline{CA + B}}$$

b) Draw the schematic for the CMOS circuit which will implement the following function with the fewest number of transistors.

$$F = \overline{X \bullet Y + Z}$$

c) Sketch the stick diagram for the circuit in (b) and label all inputs and outputs. You may use inverted inputs in your schematic and stick diagram.

Honor Pledge

By signing below, I pledge that I have neither given nor received aid on this exam, nor have I witnessed any other student giving or receiving aid.
