CMOS Inverter: DC Analysis

- Analyze DC Characteristics of CMOS Gates by studying an Inverter

- DC Analysis
  - DC value of a signal in static conditions

- DC Analysis of CMOS Inverter
  - $V_{in}$, input voltage
  - $V_{out}$, output voltage
  - single power supply, $V_{DD}$
  - Ground reference
  - find $V_{out} = f(V_{in})$

- Voltage Transfer Characteristic (VTC)
  - plot of $V_{out}$ as a function of $V_{in}$
  - vary $V_{in}$ from 0 to $V_{DD}$
  - find $V_{out}$ at each value of $V_{in}$

\[ pFET: \quad V_{TP} < 0 \]
\[ \beta_p = k_p \left( \frac{W}{L} \right)_p \]

\[ nFET: \quad V_{TN} > 0 \]
\[ \beta_n = k_n \left( \frac{W}{L} \right)_n \]
Inverter Voltage Transfer Characteristics

- **Output High Voltage, \( V_{OH} \)**
  - maximum output voltage
  - occurs when input is low (\( V_{in} = 0 \)V)
  - pMOS is ON, nMOS is OFF
  - pMOS pulls \( V_{out} \) to \( V_{DD} \)
  - \( V_{OH} = V_{DD} \)

- **Output Low Voltage, \( V_{OL} \)**
  - minimum output voltage
  - occurs when input is high (\( V_{in} = V_{DD} \))
  - pMOS is OFF, nMOS is ON
  - nMOS pulls \( V_{out} \) to Ground
  - \( V_{OL} = 0 \) V

- **Logic Swing**
  - Max swing of output signal
  - \( V_L = V_{OH} - V_{OL} \)
  - \( V_L = V_{DD} \)
Inverter Voltage Transfer Characteristics

- **Gate Voltage, f(Vin)**
  - \( V_{GSn} = Vin, \ V_{SGp} = VDD - Vin \)

- **Drain Voltage, f(Vout)**
  - \( V_{DSn} = Vout, \ V_{SDp} = VDD - Vout \)

- **Transition Region (between \( V_{OH} \) and \( V_{OL} \))**
  - **Vin low**
    - \( Vin < Vtn \)
      - \( Mn \) in Cutoff, OFF
      - \( Mp \) in Triode, Vout pulled to VDD
    - **Vin > Vtn < ~Vout**
      - \( Mn \) in Saturation, strong current
      - \( Mp \) in Triode, \( V_{SG} \) & current reducing
      - Vout decreases via current through \( Mn \)
  - **Vin \approx \frac{1}{2} \ VDD**
    - \( Mn \) and \( Mp \) both in Saturation
    - maximum current at \( Vin = Vout \)
  - **Vin high**
    - \( Vin > ~Vout, \ Vin < VDD - |Vtp| \)
      - \( Mn \) in Triode, \( Mp \) in Saturation
    - \( Vin > VDD - |Vtp| \)
      - \( Mn \) in Triode, \( Mp \) in Cutoff

\[ +V_GSn -Vin \]
\[ +V_{SGp} -Vin \]
\[ +V_GSn -Vin \]
\[ +V_{SGp} -Vin \]
\[ +V_{SGp} -Vin \]

Vin < \( V_IL \)
input logic LOW

Vin > \( V_{IH} \)
input logic HIGH
Noise Margin

• Input Low Voltage, $V_{IL}$
  - $V_{in}$ such that $V_{in} < V_{IL} = \text{logic 0}$
  - point 'a' on the plot
    • where slope, $\frac{\partial V_{in}}{\partial V_{out}} = -1$

• Input High Voltage, $V_{IH}$
  - $V_{in}$ such that $V_{in} > V_{IH} = \text{logic 1}$
  - point 'b' on the plot
    • where slope = -1

• Voltage Noise Margins
  - measure of how stable inputs are with respect to signal interference
  - $V_{NM_H} = V_{OH} - V_{IH}$
    $= V_{DD} - V_{IH}$
  - $V_{NM_L} = V_{IL} - V_{OL}$
    $= V_{IL}$
  - desire large $V_{NM_H}$ and $V_{NM_L}$ for best noise immunity
Switching Threshold

- Switching threshold = point on VTC where $V_{out} = V_{in}$
  - also called midpoint voltage, $V_M$
  - here, $V_{in} = V_{out} = V_M$

- Calculating $V_M$
  - at $V_M$, both nMOS and pMOS in Saturation
  - in an inverter, $I_{Dn} = I_{Dp}$, always!
  - solve equation for $V_M$

\[ I_{Dn} = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GSn} - V_{in})^2 = \frac{\beta_n}{2} (V_{GSn} - V_{in})^2 = \frac{\beta_p}{2} (V_{SGp} - |V_{tp}|)^2 = I_{Dp} \]

- express in terms of $V_M$

\[ \frac{\beta_n}{2} (V_M - V_{in})^2 = \frac{\beta_p}{2} (V_{DD} - V_M - |V_{tp}|)^2 \Rightarrow \sqrt{\frac{\beta_n}{\beta_p}} (V_M - V_{in}) = V_{DD} - V_M - |V_{tp}| \]

- solve for $V_M$

\[ V_M = \frac{V_{DD} - |V_{tp}| + V_{in} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \]
Effect of Transistor Size on VTC

- Recall
  \[ \beta_n = k'_n \frac{W}{L}, \quad \frac{\beta_n}{\beta_p} = \frac{k'_n \left( \frac{W}{L} \right)_n}{k'_p \left( \frac{W}{L} \right)_p} \]

- If nMOS and pMOS are same size
  - \((W/L)_n = (W/L)_p\)
  - \(C_{oxn} = C_{oxp} \) (always)
  \[ \frac{\beta_n}{\beta_p} = \frac{\mu_n C_{oxn} \left( \frac{W}{L} \right)_n}{\mu_p C_{oxp} \left( \frac{W}{L} \right)_p} = \frac{\mu_n}{\mu_p} \cong 2 \text{ or } 3 \]

- If \( \frac{\mu_n}{\mu_p} = \left( \frac{W}{L} \right)_n \), then \( \frac{\beta_n}{\beta_p} = 1 \) since \( L \) normally min. size for all tx, can get betas equal by making \( W_p \) larger than \( W_n \)

- Effect on switching threshold
  - if \( \beta_n \approx \beta_p \) and \( V_{tn} = |V_{tp}|, \quad V_M = VDD/2, \) exactly in the middle

- Effect on noise margin
  - if \( \beta_n \approx \beta_p, \) \( V_{IH} \) and \( V_{IL} \) both close to \( V_M \) and noise margin is good
Example

- **Given**
  - $k'n = 140\mu A/V^2$, $V_{tn} = 0.7V$, $V_{DD} = 3V$
  - $k'p = 60\mu A/V^2$, $V_{tp} = -0.7V$

- **Find**
  - a) tx size ratio so that $V_M = 1.5V$
  - b) $V_M$ if tx are same size

transition pushed lower as beta ratio increases
CMOS Inverter: Transient Analysis

- Analyze Transient Characteristics of CMOS Gates by studying an Inverter

- Transient Analysis
  - signal value as a function of time

- Transient Analysis of CMOS Inverter
  - Vin(t), input voltage, function of time
  - Vout(t), output voltage, function of time
  - VDD and Ground, DC (not function of time)
  - find Vout(t) = f(Vin(t))

- Transient Parameters
  - output signal rise and fall time
  - propagation delay
**Transient Response**

- **Response to step change in input**
  - delays in output due to parasitic R & C

- **Inverter RC Model**
  - Resistances
    - \( R_n = \frac{1}{\beta_n(V_{DD}-V_{tn})} \)
    - \( R_p = \frac{1}{\beta_n(V_{DD}-|V_{tp}|)} \)
  - Output Cap. (only output is important)
    - \( C_{Dn} \) (nMOS drain capacitance)
      - \( C_{Dn} = \frac{1}{2} \cdot \text{Cox} \cdot W_n \cdot L + C_j \cdot A_{Dnbot} + C_{jsw} \cdot P_{Dnsw} \)
    - \( C_{Dp} \) (pMOS drain capacitance)
      - \( C_{Dp} = \frac{1}{2} \cdot \text{Cox} \cdot W_p \cdot L + C_j \cdot A_{Dpbot} + C_{jsw} \cdot P_{Dpsw} \)
  - Load capacitance, due to gates attached at the output
    - \( C_L = 3 \cdot C_{in} = 3 \cdot (C_{Gn} + C_{Gp}) \), 3 is a “typical” load
  - Total Output Capacitance
    - \( C_{out} = C_{Dn} + C_{Dp} + C_L \)

term “fan-out” describes # gates attached at output
Fall Time

- Fall Time, $t_f$
  - time for output to fall from '1' to '0'

- derivation:
  \[ i = -C_{out} \frac{\partial V_{out}}{\partial t} = \frac{V_{out}}{R_n} \]

  - initial condition, $V_{out}(0) = V_{DD}$
  - solution
    \[ V_{out}(t) = V_{DD} e^{-t/\tau_n} \]

  \[ t = \tau_n \ln \left( \frac{V_{DD}}{V_{out}} \right) \]

- definition
  - $t_f$ is time to fall from 90% value $[V_1,t_x]$ to 10% value $[V_0,t_y]$

  \[ t = \tau_n \ln \left( \frac{V_{DD}}{0.1V_{DD}} \right) - \ln \left( \frac{V_{DD}}{0.9V_{DD}} \right) \]

  \[ t_f = 2.2 \tau_n \]
Rise Time

- Rise Time, \( t_r \)
  - time for output to rise from '0' to '1'
  - derivation:
    \[
    i = C_{out} \frac{\partial V_{out}}{\partial t} = \frac{V_{DD} - V_{out}}{R_p}
    \]
    - initial condition, \( V_{out}(0) = 0V \)
    - solution
    \[
    V_{out}(t) = V_{DD} \left[ 1 - e^{-t/\tau_p} \right]
    \]
    - definition
      - \( t_f \) is time to rise from 10% value \([V_0, t_u]\) to 90% value \([V_1, t_v]\)
      - \( t_r = 2.2 \tau_p \)

- Maximum Signal Frequency
  - \( f_{max} = 1/(t_r + t_f) \)
  - faster than this and the output can't settle
**Propagation Delay**

- Propagation Delay, $t_p$
  - measures speed of output reaction to input change
  - $t_p = \frac{1}{2} (t_{pf} + t_{pr})$
- Fall propagation delay, $t_{pf}$
  - time for output to fall by 50%
    - reference to input change by 50%
- Rise propagation delay, $t_{pr}$
  - time for output to rise by 50%
    - reference to input change by 50%
- Ideal expression (if input is step change)
  - $t_{pf} = \ln(2) \tau_n$
  - $t_{pr} = \ln(2) \tau_p$
- Total Propagation Delay
  - $t_p = 0.35(\tau_n + \tau_p)$

Propagation delay measurement:
- from time input reaches 50% value
- to time output reaches 50% value

Add rise and fall propagation delays for total value
Switching Speed - Resistance

- **Rise & Fall Time**
  - $t_f = 2.2 \tau_n$, $t_r = 2.2 \tau_p$.

- **Propagation Delay**
  - $t_p = 0.35(\tau_n + \tau_p)$

- **In General**
  - Delay $\propto \tau_n + \tau_p$
  - $\tau_n + \tau_p = Cout \ (R_n + R_p)$

- **Define delay in terms of design parameters**
  - $R_n + R_p = (V_{DD} - V_t) (\beta_n + \beta_p)$
    - $\beta_n \beta_p (V_{DD} - V_t)^2$
  - $R_n + R_p = \frac{\beta_n + \beta_p}{\beta_n \beta_p (V_{DD} - V_t)}$

  - if $V_t = Vtn = |Vtp|$

  - $\tau_n = R_n C_{out}$
  - $\tau_p = R_p C_{out}$

- **Beta Matched** if $\beta_n = \beta_p = \beta$
  - $R_n + R_p = \frac{2}{\beta (V_{DD} - V_t)} = \frac{2 L}{\mu_\text{Cox} W (V_{DD} - V_t)}$

- **Width Matched** if $W_n = W_p = W$, and $L = L_n = L_p$
  - $R_n + R_p = \frac{L (\mu_n + \mu_p)}{(\mu_n \mu_p) \text{Cox} W (V_{DD} - V_t)}$

- **To decrease R's**, $\downarrow L$, $\uparrow W$, $\uparrow VDD$, ( $\uparrow \mu_p$, $\uparrow \text{Cox}$)
Switching Speed - Capacitance

- From Resistance we have
  - $\downarrow L$, $\uparrow W$, $\uparrow VDD$, ($\uparrow \mu_p$, $\uparrow \text{Cox}$)
  - but $\uparrow VDD$ increases power
  - $\uparrow W$ increases $C_{out}$

- $C_{out}$
  - $C_{out} = \frac{1}{2} \text{Cox} \cdot L \cdot (W_n+W_p) + C_j \cdot 2L$
  - $C_{out} \approx L \cdot (W_n+W_p) \cdot [3\frac{1}{2} \text{Cox} + 2 \cdot C_j]$
  - $C_{out} \propto L \cdot (W_n+W_p)$

- To decrease $C_{out}$, $\downarrow L$, $\downarrow W$, ($\downarrow C_j$, $\downarrow \text{Cox}$)

- Delay $\propto C_{out}(R_n+R_p) \propto L \cdot W \cdot \frac{L}{W \cdot VDD} = \frac{L^2}{VDD}$

Decreasing $L$ (reducing feature size) is best way to improve speed!
Switching Speed - Local Modification

- Previous analysis applies to the overall design
  - shows that reducing feature size is critical for higher speed
  - general result useful for creating cell libraries

- How do you improve speed within a specific gate?
  - increasing W in one gate will not increase $C_G$ of the load gates
    - $C_{out} = C_{Dn} + C_{Dp} + C_L$
    - increasing W in one logic gate will increase $C_{Dn/p}$ but not $C_L$
      - $C_L$ depends on the size of the tx gates at the output
      - as long as they keep minimum W, $C_L$ will be constant
  - thus, increasing W is a good way to improve the speed within a local point
  - But, increasing W increases chip area needed, which is bad
    - fast circuits need more chip area (chip “real estate”)

- Increasing VDD is not a good choice because it increases power consumption
CMOS Power Consumption

- \( P = P_{\text{DC}} + P_{\text{dyn}} \)
  - \( P_{\text{DC}} \): DC (static) term
  - \( P_{\text{dyn}} \): dynamic (signal changing) term

- \( P_{\text{DC}} \)
  - \( P = I_{\text{DD}} V_{\text{DD}} \)
    - \( I_{\text{DD}} \): DC current from power supply
    - ideally, \( I_{\text{DD}} = 0 \) in CMOS: ideally only current during switching action
    - leakage currents cause \( I_{\text{DD}} > 0 \), define quiescent leakage current, \( I_{\text{DDQ}} \) (due largely to leakage at substrate junctions)
  - \( P_{\text{DC}} = I_{\text{DDQ}} V_{\text{DD}} \)

- \( P_{\text{dyn}} \), power required to switch the state of a gate
  - charge transferred during transition, \( Q_e = C_{\text{out}} V_{\text{DD}} \)
  - assume each gate must transfer this charge 1x/clock cycle
  - \( P_{\text{average}} = V_{\text{DD}} Q_e f = C_{\text{out}} V_{\text{DD}}^2 f \), \( f \) = frequency of signal change

- Total Power, \( P = I_{\text{DDQ}} V_{\text{DD}} + C_{\text{out}} V_{\text{DD}}^2 f \)

Power increases with \( C_{\text{out}} \) and frequency, and strongly with \( V_{\text{DD}} \) (second order).
Multi-Input Gate Signal Transitions

• In multi-input gates multiple signal transitions produce output changes

• What signal transitions need to be analyzed?
  - for a general N-input gate with $M_0$ low output states and $M_1$ high output states
    • # high-to-low output transitions = $M_0 \cdot M_1$
    • # low-to-high output transitions = $M_1 \cdot M_0$
    • total transitions to be characterized = $2 \cdot M_0 \cdot M_1$
    • example: NAND has $M_0 = 1$, $M_1 = 3$
  - don’t test/characterize cases without output transitions

• Worst-case delay is the slowest of all possible cases
  - worst-case high-to-low
  - worst-case low-to-high
  - often different input transitions for each of these cases
Series/Parallel Equivalent Circuits

- Scale both $W$ and $L$
  - no effective change in $W/L$
  - increases gate capacitance

inputs must be at same value/voltage

- **Series Transistors**
  - increases effective $L$

- **Parallel Transistors**
  - increases effective $W$

\[
\beta = \mu \text{Cox} \cdot \frac{W}{L}
\]
### NAND: DC Analysis

- **Multiple Inputs**
- **Multiple Transitions**
- **Multiple VTCs**
  - VTC varies with transition
    - transition from 0,0 to 1,1 pushed right of others
    - why?
  - \( V_M \) varies with transition
    - assume all tx have same \( L \)
    - \( V_M = V_A = V_B = V_{out} \)
      - can merge transistors at this point
    - if \( W_{PA} = W_{PB} \) and \( W_{NA} = W_{NB} \)
      - series nMOS, \( \beta_N \Rightarrow \frac{1}{2} \beta_n \)
      - parallel pMOS, \( \beta_P \Rightarrow 2 \beta_p \)
  - can now calculate the NAND \( V_M \)
NAND Switching Point

- Calculate VM for NAND
  - 0,0 to 1,1 transition
    - all tx change states (on, off)
    - in other transitions, only 2 change
  - \( V_M = V_A = V_B = V_{out} \)
  - set \( I_{Dn} = I_{Dp} \), solve for \( V_M \)
    \[
    V_M = \frac{VDD - |V_p| + V_m \frac{1}{2} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{2} \sqrt{\frac{\beta_n}{\beta_p}}}
    \]
  - denominator reduced more
    - VTC shifts right
    - series nMOS means more resistance to output falling, shifts VTC to right
    - to balance this effect and set \( V_M \) to \( V_{DD}/2 \), can increase \( \beta \) by increasing \( W_n \)

- For NAND with \( N \) inputs
  \[
  V_M = \frac{VDD - |V_p| + V_m \frac{1}{N} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{N} \sqrt{\frac{\beta_n}{\beta_p}}}
  \]

but, since \( \mu_n > \mu_p \), \( V_M \approx V_{DD}/2 \) when \( W_n = W_p \)
NOR: DC Analysis

- Similar Analysis to NAND
- Critical Transition
  - 0,0 to 1,1
  - when all transistors change
- $V_M$ for NOR2 critical transition
  - if $W_{pA}=W_{pB}$ and $W_{nA}=W_{nB}$
    - parallel nMOS, $\beta_n \Rightarrow 2 \beta_n$
    - series pMOS, $\beta_p \Rightarrow \frac{1}{2} \beta_p$

$$V_M = \frac{V_{DD} - |V_p| + 2V_{m} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + 2 \sqrt{\frac{\beta_n}{\beta_p}}}$$

for NOR2

$$V_M = \frac{V_{DD} - |V_p| + NV_{m} \sqrt{\beta_n/\beta_p}}{1 + N \sqrt{\beta_n/\beta_p}}$$

for NOR-N

- series pMOS resistance means slower rise
- VTC shifted to the left
  - to set $V_M$ to $V_{DD}/2$, increase $W_p$
    - this will increase $\beta_p$
**NAND: Transient Analysis**

- **NAND RC Circuit**
  - \( R \): standard channel resistance
  - \( C \): \(C_{\text{out}} = C_L + C_{\text{Dn}} + 2C_{\text{Dp}}\)

- **Rise Time, \( t_r \)**
  - Worst case charge circuit
    - \( t_r = 2.2 \ \tau_p \)
    - \( \tau_p = R_p \ C_{\text{out}} \)
  - Best case charge circuit
    - \( 2 \) pMOS ON, \( R_p \Rightarrow R_p/2 \)

- **Fall Time, \( t_f \)**
  - Discharge Circuit
    - \( 2 \) series nMOS, \( R_n \Rightarrow 2R_n \)
    - must account for internal cap, \( C_x \)
  - \( t_f = 2.2 \ \tau_n \)
    - \( \tau_n = C_{\text{out}} (2 \ R_n) + C_x \ R_n \)

\[
\begin{align*}
C_x &= C_{\text{Sn}} + C_{\text{Dn}}
\end{align*}
\]
NOR: Transient Analysis

- **NOR RC Circuit**
  - R: standard channel resistance
  - C: \( C_{out} = C_L + 2C_{Dn} + C_{Dp} \)

- **Fall Time, \( t_f \)**
  - Worst case discharge circuit
    - 1 nMOS ON
    - \( t_f = 2.2 \tau_n \)
      - \( \tau_n = R_n \ C_{out} \)
    - best case discharge circuit
      - 2 nMOS ON, \( R_n \Rightarrow R_n/2 \)

- **Rise Time, \( t_r \)**
  - Charge Circuit
    - 2 series pMOS, \( R_p \Rightarrow 2R_p \)
      - must account for internal cap, \( C_y \)
    - \( t_r = 2.2 \tau_p \)
      - \( \tau_p = C_{out} \ (2 \ R_p\ ) + C_y \ R_p \)

\[ C_y = C_{Sp} + C_{Dp} \]
NAND/NOR Performance

- Inverter: symmetry ($V_M = V_{DD}/2$), $\beta_n = \beta_p$
  - $(W/L)_p = \frac{\mu_n}{\mu_p} (W/L)_n$
- Match INV performance with NAND
  - pMOS, $\beta_p = \beta_p$, same as inverter
  - nMOS, $\beta_N = 2\beta_n$, to balance for 2 series nMOS
- Match INV performance with NOR
  - pMOS, $\beta_p = 2 \beta_p$, to balance for 2 series pMOS
  - nMOS, $\beta_N = \beta_n$, same as inverter
- NAND and NOR will still be slower due to larger $C_{out}$
- This can be extended to 3, 4, ... $N$ input NAND/NOR gates

$\beta$ is adjusted by changing transistor size (width)
NAND/NOR Transient Summary

• **Critical Delay Path**
  - paths through series transistors will be slower
  - more series transistors means worse delays

• **Tx Sizing Considerations**
  - increase $W$ in series transistors
  - balance $\beta_n/\beta_p$ for each cell

• **Worst Case Transition**
  - when all series transistor go from OFF to ON
  - and all internal caps have to be
    - charged (NOR)
    - discharged (NAND)
Performance Considerations

- Speed based on $\beta_n$, $\beta_p$ and parasitic caps
- DC performance ($V_M$, noise) based on $\beta_n/\beta_p$
- Design for speed not necessarily provide good DC performance
- Generally set tx size to optimize speed and then test DC characteristics to ensure adequate noise immunity

- Review Inverter: Our performance reference point
  - for symmetry ($V_M = V_{DD}/2$), $\beta_n = \beta_p$
    - which requires $(W/L)_p = \mu_n/\mu_p (W/L)_n$
  - Use inverter as reference point for more complex gates

- Apply slowest arriving inputs to series node closest to output
  - let faster signals begin to charge/discharge nodes closer to VDD and Ground
Timing in Complex Logic Gates

- **Critical delay path** is due to series-connected transistors
  - Example: \( f = x(y + z) \)
    - assume all tx are same size
  - Fall time critical delay
    - worst case, \( x \) ON, and \( y \) or \( z \) ON
    - \( t_f = 2.2 \tau_n \)
      - \( \tau_n = R_n C_n + 2 R_n C_{out} \)
      - \( C_{out} = 2C_{Dp} + C_{Dn} + C_L \)
      - \( C_n = 2C_{Dn} + C_{Sn} \)
  - Rise time critical delay
    - worst case, \( y \) and \( z \) ON, \( x \) OFF
    - \( t_r = 2.2 \tau_p \)
      - \( \tau_p = R_p C_p + 2 R_p C_{out} \)
      - \( C_{out} = 2C_{Dp} + C_{Dn} + C_L \)
      - \( C_p = C_{Dp} + C_{Sp} \)

size vs. tx speed considerations

\( \uparrow Wnx \Rightarrow \downarrow Rn \) but \( \uparrow Cout \) and \( \uparrow Cn \)
\( \downarrow Wny \Rightarrow \downarrow Cn \) but \( \uparrow Rn \)

\( \uparrow Wpz \Rightarrow \downarrow Rp \) but \( \uparrow Cout \) and \( \uparrow Cp \)
\( \downarrow Wpx \Rightarrow \) no effect on critical path
Sizing in Complex Logic Gates

• Improving speed within a single logic gate

• An Example: \( f = (a \ b + c \ d) \times \)

• nMOS
  - discharge through 3 series nMOS
  - set \( \beta_N = 3\beta_n \)

• pMOS
  - charge through 2 series pMOS
  - set \( \beta_P = 2\beta_p \)
  - but, \( M_p - x \) is alone so \( \beta_{P1} = \beta_p \)
    • but setting \( \beta_{P1} = 2\beta_p \) might make layout easier

• These large transistors will increase capacitance and layout area and may only give a small increase in speed

• Advanced logic structures are best way to improve speed
Timing in Multi-Gate Circuits

- What is the worst-case delay in multi-gate circuits?
  - too many transitions to test manually
- Critical Path
  - longest delay through a circuit block
  - largest sum of delays, from input to output
  - intuitive analysis: signal that passes through most gates
    - not always true. can be slower path through fewer gates

path through most gates

critical path if delay due to D input is very slow
Power in Multi-Input Logic Gates

- **Inverter Power Consumption**
  - \( P = P_{DC} + P_{dyn} = V_{DD}I_{DDQ} + C_{out}V^2_{DD}f \)
  - Assumes gates switches output state once per clock cycle, \( f \)

- **Multi-Input Gates**
  - Same DC component as inverter, \( P_{DC} = V_{DD}I_{DDQ} \)
  - For dynamic power, need to estimate “activity” of the gate, how often will the output be switching
  - \( P_{dyn} = aC_{out}V^2_{DD}f \), \( a = \) activity coefficient
  - Estimate activity from truth table
    - \( a = p_0 p_1 \)
    - \( p_0 = \) prob. output is at 0
    - \( p_1 = \) prob. of transition to 1
Timing Analysis of Transmission Gates

- TG = parallel nMOS and pMOS

- RC Model
  - in general, only one tx active at same time
    - nMOS pulls output low
    - pMOS pushes output high
  - $R_{TG} = \text{max} \ (R_n, R_p)$
  - $C_{in} = C_{Sn} + C_{Dp}$
    - if output at higher voltage than input
  - larger $W$ will decrease $R$ but increase $C_{in}$

- Note: no connections to VDD-Ground. Input signal, $V_{in}$, must drive TG output; TG just adds extra delay
Pass Transistor

• Single nMOS or pMOS tx
• Often used in place of TGs
  - less area and wiring
  - can’t pull to both VDD and Ground
  - typically use nMOS for better speed

• Rise and Fall Times
  - $\tau_n = R_n \cdot C_{out}$
  - $t_f = 2.94 \cdot \tau_n$
  - $t_r = 18 \cdot \tau_n$
    - much slower than fall time
  - $\Phi = 1$

• nMOS can’t pull output to VDD
  - rise time suffers from threshold loss in nMOS