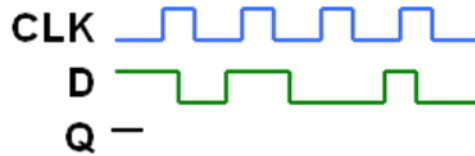


Due Mon Jan 14 at the beginning of class.

These problems must be done by hand, without the use of a conversion program or calculator. Please show as much of your work as necessary to demonstrate that you have worked through these problems manually.

1. Determine the Hexadecimal and Decimal values for each of the following Binary numbers.
 - a. 10011110
 - b. 01011001
 - c. 11010100
2. Determine the Binary and Hexadecimal values for each of the following Decimal numbers. Assume all values can be represented by 4 binary bits.
 - a. 3
 - b. 12
 - c. 15
3. Determine the binary 2's complement for each of the following 8-bit numbers:
 - a. 11111110
 - b. 00000000
 - c. 00010000
4. Determine the base-10 value of the following 8-bit signed 2's complement numbers:
 - a. 01000101
 - b. 10111011
 - c. 11111111
5. Express each of the following base-10 numbers as 4-bit binary numbers in signed 2's complement form:
 - a. -4
 - b. 9
 - c. -7
6. What is the largest negative 8-bit signed 2's complement value in binary notation? What is the largest positive value? What are the decimal equivalents of these values?
7. Assume the following are 4-bit signed 2's complement numbers. Perform the specified arithmetic. For each problem, determine if a 2's complement overflow has occurred. Check each problem by performing the same operations in decimal form.
 - a. $1010 + 0111$
 - b. $0101 - 1110$
 - c. $1000 - 0101$
8. Assume the following are 8-bit signed 2's complement numbers specified in hexadecimal. Determine the arithmetic result. You will probably want to convert to binary to determine the sign of each 2's complement value. Give your answer in hexadecimal notation. Check each problem by performing the same operations in decimal notation. If 2's complement overflow occurs, show how it can be detected.
 - a. $E4 + 03$
 - b. $E5 - EE$
 - c. $DA - DB$

9. Minimize the function $F = AB + \overline{A}\overline{B} + ABC$ using your choice of min/max terms, K-maps or Boolean arithmetic. The reduced function should require the least possible number of operations (AND/OR).
10. Show using gate schematics that INV (NOT), OR and AND logic functions can be implemented using only NAND gates.
11. The timing diagram for the clock (CLK) and data (D) inputs to a D-type flip flop are shown below. Draw the output (Q) if the DFF is negative edge triggered. Assume Q starts hi.



12. The contents (stored data) of a 4-bit register are shown below. Assume a shift operation loads in a 0 value. Show the contents of each register after:
 - a. a shift right by 1 operation
 - b. a rotate left by 2 operation

