Timeline of Computer History Highlights

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~ 2000 B.C. ~ 500 B.C.	Sumer (Sumerian) China	Abacus -First calculating machine
~1650 A.D.	Wilhelm Schickard (and others including Blaise Pascal)	First mechanical adder/subtractor (not programmable)
1837	Charles Babbag	First concept and design a fully programmable mechanical computer
1937	Alan Turing	Concept of the algorithm and computation with the Turing machine
1940s (WWII)		First plans for an electrical computer (not planned for personal use)
1950	John Mauchly and J. Presper Eckert (University of Pennsylvania, U.S. Army)	ENIAC (Electronic Numerical Integrator and Computer) –First general-purpose electronic computer using relay memories and vacuum tubes
1948	William Shockley et.al. (Bell Labs)	First semiconductor transistor; the beginning of the microelectronics age
1958	Jack Kilby (Texas Instruments) won Nobel Prize in 2000	First integrated circuit (multiple transistors in one substrate); built in germanium
1959	Robert Noyce (Fairchild Semiconductor)	First silicon integrated circuit
1971	Intel	Intel 4004 (4-bit CPU) -First commercial single-chip microprocessor

Pathways of Computing

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Computer hardware developed in two distinct paths

- Microprocessor
  - general purpose computer: fast & computationally powerful
  - EX: PCs, servers, etc.

- Microcontroller
  - "embedded" controller: compact, inexpensive, extensive I/O interfaces
  - EX: cameras, cars, etc.

Embedded system: electronic system with microcontroller and in-module I/O devices, especially sensors/actuators

- modern embedded system may have both microcontrollers (control & I/O) and microprocessors (computation)

Basic Computer Organization

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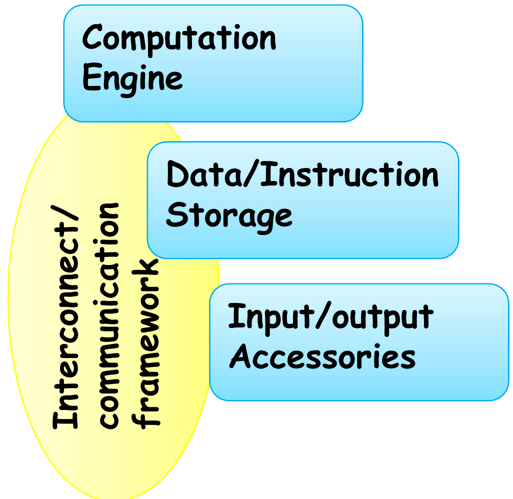
- What are the necessary elements of a computing machine?



Basic Computer Architecture

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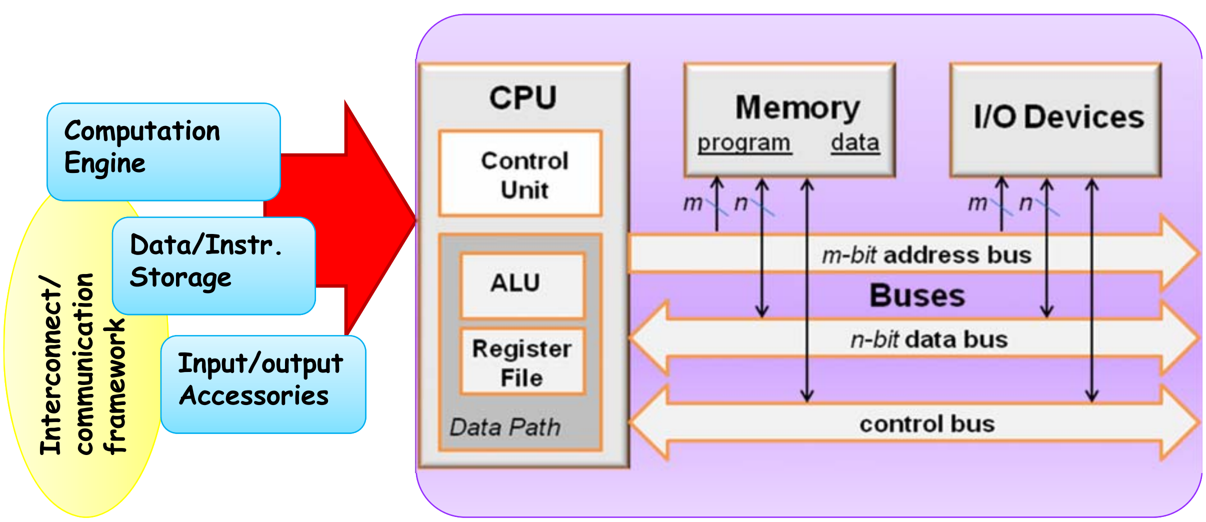
- Stored-program computer
  - A.K.A. von Neumann architecture



Computer Architecture

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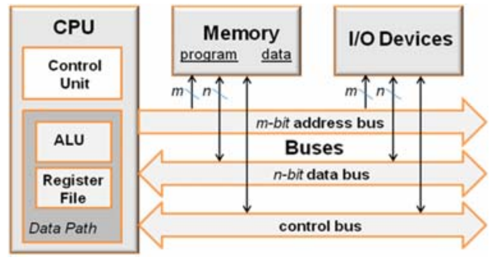
* Fundamental components of microcontrollers and microprocessors



- **Memory**
  - Storage for instructions and data
  - Many different types of memory (more later)
    - EX: *cache* : small, quickly accessed
- **I/O Devices**
  - Interfaces to the outside world
    - EX: *inputs* : keyboard, mouse, mic, scanner
    - EX: *outputs* : monitor/display, speaker, printer
- **Buses**
  - Physical connections between CPU, Memory and I/O
  - 3 bus types
    - address, data, control
- CPU central processing unit
  - governs order of instruction execution, controls access to memory and I/O, preforms arithmetic and logic (ALU) , etc.
  - contains ALU, control unit, registers, timers and internal buses
  - speed set by clock (e.g. 1MHz, 2.4GHz)

Central Processing Unit

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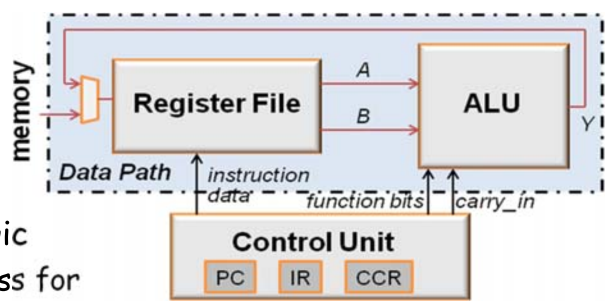
Functional structure of CPU

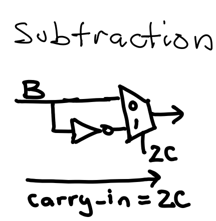


*** Control Unit**

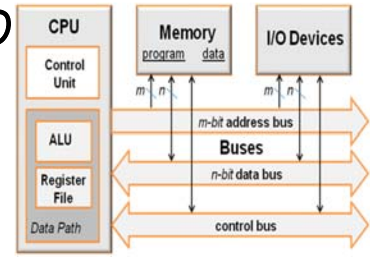
- decodes instructions & monitors instruction execution
- contains hardware instruction logic
  - Program Counter (PC) : holds address for next instructions
  - Instruction Register (IR): holds current instruction
  - Condition Code Register (CCR): holds "flags" generated by past instructions
  - Stack Pointer (SP) : holds address of last value on stack

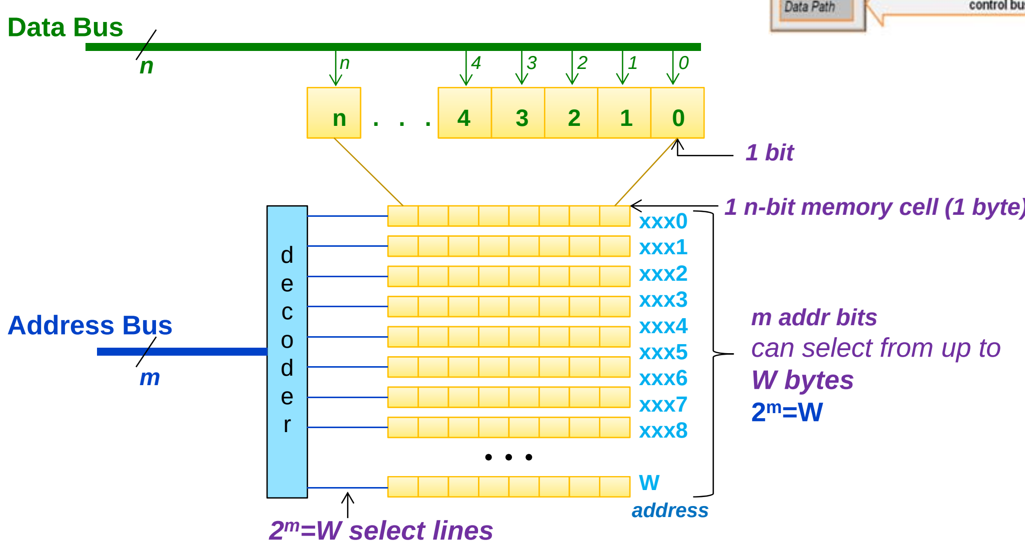
*** Datapath**: ALU + Register file

- ALU : arithmetic – logic unit, executes instructions
  - EX : Add, AND, Move data
  - "size" of ALU determines how many bits processed at once
    - EX: 8-bit, 16-bit, 32-bit word length
- Register file : small internal memory, temporary data (data or memory address) storage



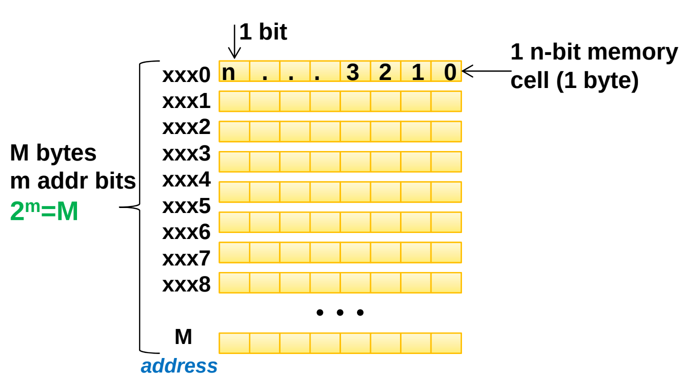
- Bus: connects CPU to Memory & I/O
  - n-bit Data bus: n-bits of parallel data lines
  - m-bit Memory bus: m-bits of parallel addr. lines
    - can access $W=2^m$ individual addresses





- Consider a μC with n-bit ALU and m-bit memory address bus ***generally, #ALU bits = #bits per memory cell***
  - If n = 16 and m = 32
    - how many bits in each cell (aka, byte or word)?
    - how many cells (bytes) can be addressed?
    - how many total bits can be stored?
  - What is 'm' if we can access 1M-bytes memory?

- Useful Note:
  - 2^{10} = 1,024 = 1K
  - 2^{20} = 1M (million
  - 2^{30} = 1G (billion)



Freescale HC12/S12 Family

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- 68HC12 (6800) Family
  - 8-bit ALU
  - 16-bit memory address
  - 8 & 16-bit register file blocks and instructions
  - I/O varies with model
- HC12A4 (MC68HC812A4: schematic on next slide)
  - Components: CPU, Memory, Buses, Peripheral I/O devices
  - Baseline version discussed in lecture
- HCS12 (MCS12DP256B: schematic on following slide)
  - Version used in lab; had "advanced" functions we will ignore
  - Components
    - Memory: 25K flash EEPROM, 4K EEPROM, 12K RAM
      - RAM loses data without power (i.e., is volatile); EEPROM is non volatile
    - I/O: 89 digital input/output signals (incld 16-bit memory expansion port)
    - Peripheral blocks: 2@8-channel A/D, Timer, Pulse width module
    - Communication busses: SCI, SPI, I^2C, CAN

Detailed General Computer Architecture

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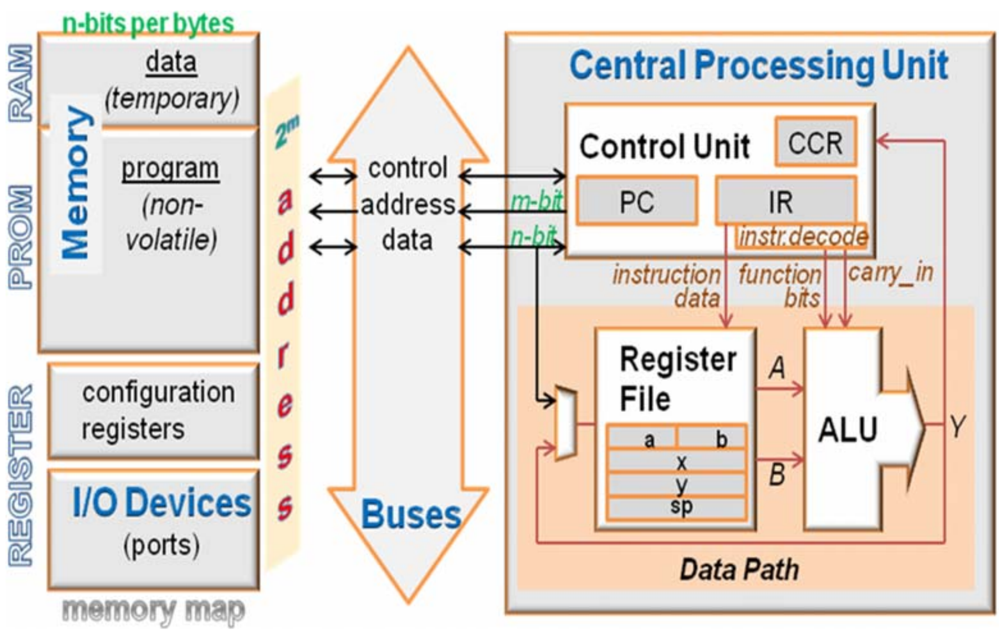
- General structure of 68HC12



Freescale HC12 Block Diagram (MC68HC812A4)

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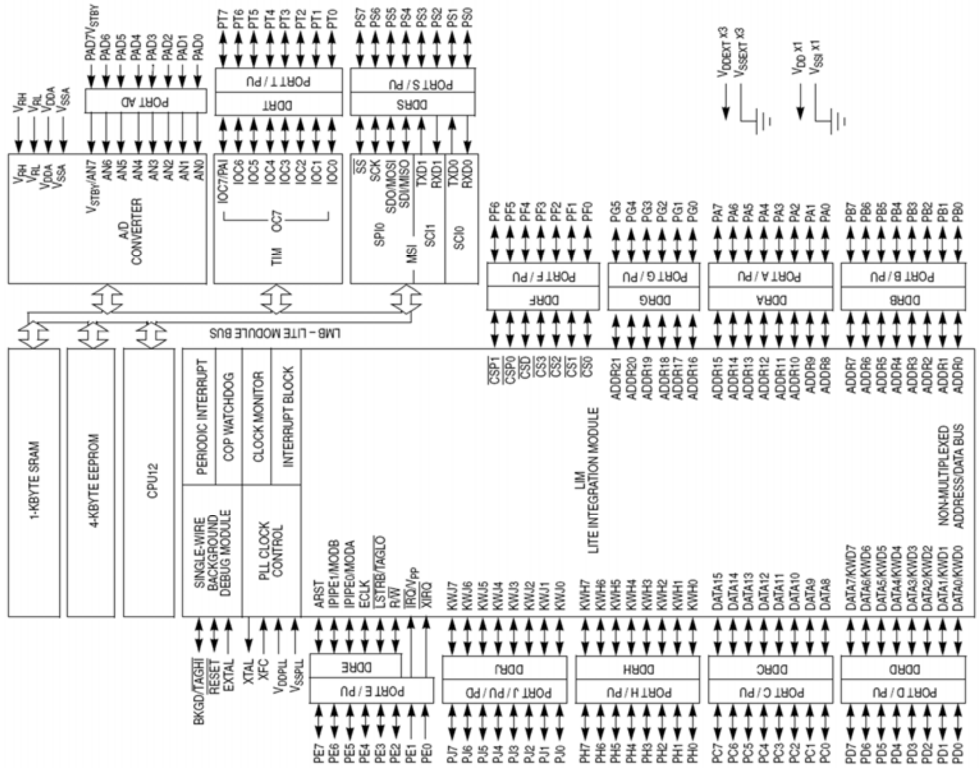

Freescale HCS12 Block Diagram (MCS12DP256B)

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