Lab 1: Cadence Virtuoso Introduction

Summary:
In this lab, students will learn how to use Cadence *Virtuoso* and construct logic gates from a basic gate library.

Learning Objectives:

- Experience designing digital circuits with Cadence *Virtuoso*
- Experience running simulations with *Virtuoso*

Resources and Supplies:

- *Cadence Virtuoso Setup Guide**
- *Cadence Virtuoso Logic Gates Tutorial**
- Eye protection (required!)

All documents* are available on the class website

Important Reminders:

- You must have ***eye protection*** to enter the lab, and you must wear eye protection while performing any task other than using the computer. This includes soldering, wire cutting, wire stripping, etc. Students without eye protection will not be allowed to work on the lab. Normal eye glasses are permitted, but safety goggles are more much effective and strongly preferred. If you do not already own eye protection, safety goggles can be purchased for a modest cost at the MSU bookstore. Eye protection is **required** for admittance to the lab.
- Pre-lab assignments must be completed before coming to the lab. Pre-lab assignments will typically require printing a pre-lab check-off sheet and completing some tasks. The completed pre-lab check-off sheet should be submitted to the lab TA before starting the in-lab assignment. If the pre-lab material is needed to complete the lab assignment (e.g., a drawn schematic), please show the check-off sheet to the TA, ask him/her to sign it to confirm they have seen it, and then submit it with your lab report.

Pre-lab Assignment:
Each student must complete his/her own pre-lab before coming to the lab. Pre-lab check-off sheets must be turned in to the TA before starting the lab assignment.

1. Read the **Important Reminders** and **Background** sections of this lab assignment.
2. Print the pre-lab sheet near the end of this document, perform the required tasks, and sign (initial) where indicated.
3. Read through the entire **Laboratory Assignment** section so you know what to expect in the lab.

Background:

Cadence Tools:

Cadence tools are a suite of CAD tools that puts circuit elements into a 2D-object form for the user to manipulate and then translates the design to a netlist that can be run through a simulation program. If you are familiar with SPICE, then a 2D object in Cadence *Virtuoso* would be equivalent to a single line in a PSPICE file, such as a voltage source. These objects can literally represent almost any type of electronic device that can be built.

Starting out with the basic elements such as transistors, capacitors, resistors, and various sources, larger more complex objects such as digital gates can be built using modern circuit design CAD tools like the Cadence software suite. The basic circuit elements are contained in *libraries* that are organized by part type, function, or project. To create a circuit design, users will *instantiate* (add a copy of) library elements into a new schematic file. New designs will be created in a library chosen by the user, for example a library created for a specific class. When a new design it completed, a *symbol* of the new design can be created. These symbols can be instantiated into new designs just like the elements from the basic cell library. This allows the user to create increasingly complex circuits using what is called a *hierarchical design method* wherein each level of the design is more complex by instantiating lower level circuits. Before any newly designed circuit is considered to be complete, its operation should be tested using a circuit simulation program, like SPICE, to determine its function and performance. Cadence *Virtuoso* provides both a graphic interface for creating schematics using 2D objects as well as a simulation engine to test circuits and display simulation results.

Making Logic Gates from Other Logic Gates:

Within Virtuoso you will find an ECE331 library containing a set of basic logic gates. These gates were themselves created by instantiating transistors in the correct manner to produce the behavior for the given gate. In ECE331, we will do only gate-level design, building circuits composed of the logic gates in the supplied ECE331 library. These include a NOR, NAND, INV, and 2:1 MUX. From these starter gates, you will be building an AND, OR, XOR and 4:1 MUX gates to expand the library. For example, Figure 1 shows one possible schematic for implementing the XOR function. In later labs, you will use these basic gates to design more complex circuits, from an adder all the way to a simple 8-bit ALU.

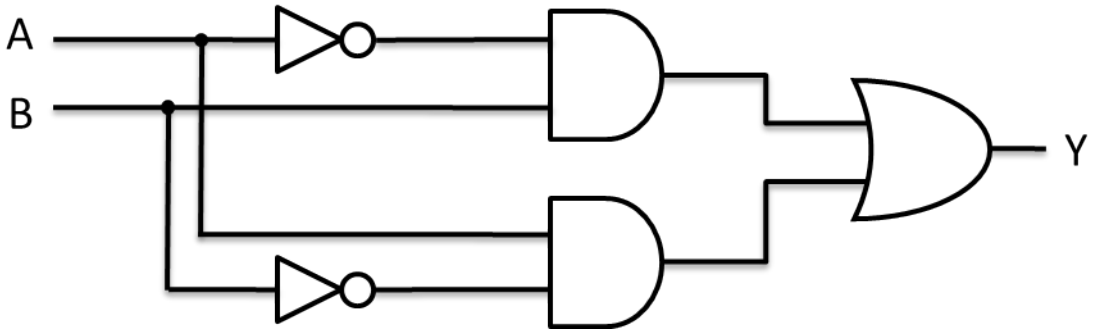


Figure 1. Schematic for a XOR gate composed of gates in the ECE331 library.

Laboratory Assignment:
This lab consists of two parts. A check-off sheet is included at the end of this lab document to record your design work and results. After you successfully finish each part of the lab, show the TA your results and ask him/her to sign the check-off sheet.

- Print the check-off sheet.

Part 1: Virtuoso Intro
In this part you will use logic gates in the ECE331 library to construct other logic gates.

1. Follow the *Cadence Virtuoso Logic Gates Tutorial* document in which you will step through the process of designing, implementing, and testing an AND gate from the gates in the *ECE331* library.

Demonstration:

2. For check off, show the TA the AND symbol, schematic, and results graph in *Virtuoso*. Do not continue until the TA has checked off Part 1 of your lab.

Part 2: Creating a Digital Gate Library

In part 2 you will design and test an OR, XOR and 4:1MUX gate following the steps in the *Cadence Logic Gates Virtuoso Tutorial*.

Design

1. Using the designated area in the check-off sheet, sketch a diagram of an OR logic circuit that uses only INV, NAND, NOR, 2:1MUX gates, which are the gates available in the ECE331 digital gate library for Cadence *Virtuoso*.
2. Repeat step 1 for a 4:1 MUX.

Implementation in Cadence Virtuoso

3. Launch *Virtuoso* from your ECE331 directory. Use the *Cadence Virtuoso Setup Guide* if you have any questions.
4. Open your *ECE331* library and create a new cellview for an OR gate.
5. Using the OR schematic from Step 1, construct the circuit in *Virtuoso*. Use the *Cadence Virtuoso Logic Gates Tutorial* if necessary.
6. Check and save (the floppy disc icon with the green check mark) the OR schematic.
7. Create a symbol for the OR gate and save it.
8. Repeat steps 4-7 for a 4:1MUX.
9. Repeat steps 4-7 for an XOR gate. Note: an XOR schematic is given in Figure 1. There are multiple ways to design an XOR gate. Feel free to use a different design, but you can only use the initial gates from the ECE331 library and must make sure it functions correctly.

10. On the check-off sheet, fill in the theoretical (expected) outputs column of the truth tables for the OR and XOR gates.

Demonstration

11. From the ECE331 website, download the ***Lab1A.txt*** stimulus file. This file will set the gate inputs to all possible logic combinations. Use this stimulus file to simulate the functionality of the OR and XOR logic gates.
12. Next from the ECE 331 website, download ***Lab1B.txt*** stimulus file. Use this stimulus file to test the designed 4:1 MUX.
13. Record your simulation results in the truth tables on the check-off sheet and write a comment on how your simulation results compared to the expected function.
14. Print the graphs from all 3 simulations. Instructions on how to print out a graph are in the *Cadence Virtuoso Logic Gates Tutorial*. If the signal names are not readable after printing out, label them with a pencil or pen. Attach these graphs to the lab report you will turn in next week.
15. Show the TA your schematics, symbols, and simulation results for all 3 new gates and ask the TA to sign Part 2 of the lab check-off sheet.

Wrap Up

Clean up your lab bench before you exit the lab.

Note, a simple lab report is required for each ECE331 lab. Reports must be turned in to the TA during the next lab (next week). Follow the ***Lab Report Guide*** on the class website. Your check-off sheets will always be attached to your lab report, along with any other relevant pages/prints, like the simulation results from this lab. The Discussion Points below must be answered within your lab report. Each student must prepare his/her own lab report; one per person not one per lab team.

Discussion Points:
As explained in the *Lab Report Guide*, you should address these discussion points in a designated section of your report.

1. You were given a beginning logic library with four logic gates from which you would be able to create all other digital logic functions. What is the absolute minimum number of beginning logic gates needed to design all digital logic functions? Can you name these gate(s)?
2. When running the simulations, why is there a difference in time from when an input changes to when the output changes? You may not have observed it unless you zoomed in close, but it was there.
3. When running the simulation you should have noticed seemingly random spikes when the inputs and outputs change. Why do you think this occurs? Do you think it is a simulation artifact or a real response of the circuit? If a real response, what is the source of these spikes? Even if you did not see them, consider what might cause such spikes.

PRE-LAB 1 CHECK-OFF SHEET
Due: At the beginning of lab.

Student Name: _____ **Lab. Section (time):** _____

In preparation for Lab 1, complete the following steps and sign your initials on the space below confirming that you have completed each task. This ***must be completed prior to coming to lab***. This sheet should be submitted to the TA at the beginning of your assigned lab session.

Part 1: Lab Safety

1. Read the ECE lab policy Initial_____
   https://www.egr.msu.edu/eceshop/labs/general_lab.php

2. Read the ECE safety policy Initial_____
   https://www.egr.msu.edu/eceshop/labs/safety/safety.pdf

Important: You must have ***eye protection*** to enter the lab, and you must wear eye protection while performing any task other than using the computer. This includes soldering, wire cutting, wire stripping, etc. Students without eye protection will not be allowed to work on the lab. Normal eye glasses are permitted, but safety goggles are more much effective and strongly preferred. If you do not already own eye protection, safety goggles can be purchased for a modest cost at the MSU bookstore. Eye protection is **required** for admittance to the lab.

3. I have eye protection Initial_____

Note: Before beginning Lab 1, you will be asked to sign a sheet confirming you have been informed of lab safety issues.

Part 2: Setup Cadence Virtuoso

Make sure you read the lab document before you start the pre-lab, especially the Background section.

1. Complete all of the steps in the *Cadence Virtuoso Setup Guide* posted on the class website.
2. Print screen capture of your PuTTY and Virtuoso windows to bring to the lab and show the TA you have completed this pre-lab task.
3. Note any questions you might want to ask the TA regarding use of Virtuoso.

TA Sign Off

TA has received this pre-lab check-off sheet and confirmed eye protection and Cadence setup.

(Initial)_____

LAB 1 CHECK-OFF SHEET

Student Name: _____ **Lab. Section (time):** _____

Part 1: ***Tutorial***

AND

		Theoretical	Simulated
A	B	Y	Y
0	0		
0	1		
1	0		
1	1		

Part 1: TA sign off Initials_____

Part 2: ***Gate Library***

Step 2-3. Record your designs in the boxes.

OR Gate

4:1 MUX

Step 10-13. Fill out the truth tables with the results.

OR

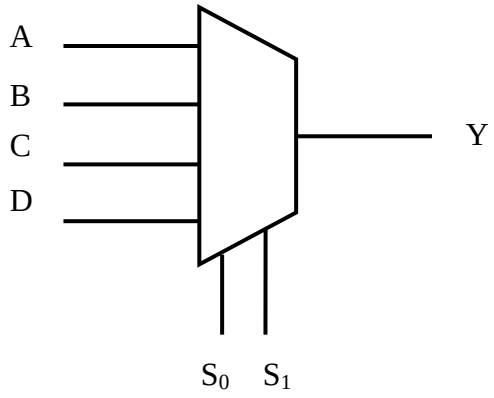
		Theoretical	Simulated
A	B	Y	Y
0	0		
0	1		
1	0		
1	1		

XOR

		Theoretical	Simulated
A	B	Y	Y
0	0		
0	1		
1	0		
1	1		

Comment:

The MUX outputs should be defined in terms of the figure below, where ***A*** is the output when the select bits are 00, etc..



S_1	S_0	Y
0	0	
0	1	
1	0	
1	1	

Comment:

Part 2: TA sign off Initials_____