A Completely Integrated, Low Noise, Low Power CMOS Frequency Synthesizer for GSM Communications

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ABSTRACT

A low power 22-mW 900MHz Frequency Synthesizer (FS), with an on-chip LC-tuned voltage controlled oscillator (VCO) for GSM applications is presented. The synthesizer possesses several novel features that include a completely integrated structure, a low phase noise on-chip LC VCO, a low-power Dual-Modulus Divider (DMD) in CML topology, a compensated charge pump with balanced switching, an on-chip third order loop filter and a proposed relatively easy to implement fractional accumulator based frequency synthesis technique. The complete synthesizer achieves in-band phase noise characteristics better than -110 dBc/Hz at 100kHz offset. The channel switching time is less than 500 μ s for a 25MHz frequency hop. The synthesizer is able to accommodate all 195 transmit and receive channels in the R-GSM band. The proposed architecture has been realized using the 0.5 μ m AMI C5N technology. The complete integrated synthesizer occupies less than 1500 $\times$ 700 μ m² of die real estate.

1. Introduction

A frequency synthesizer is a demanding mixed signal application that requires a good understanding of both analog and digital circuits. Frequency Synthesizers are usually employed in the transceiver part of various communication devices with the task of providing a stable frequency for a channel within a certain communication band. With the advancement of CMOS technology and the increase in demand of mobile devices, the realization of stable, low noise, low power and small footprint frequency synthesizers has become an industrial hot pursuit.

Frequency synthesis is needed to generate multiple signal frequencies, all derived from a common reference or time base supplied by a Temperature Compensated Crystal Oscillator (TCXO). The TCXO provides a reference frequency to the synthesizer circuit so that it may accurately produce a wide range of signals that are stable and relatively low in phase noise. For good channel selectivity a high purity carrier signal with low phase noise is required. In this paper, we propose an on chip negative g_m LC-tuned VCO with low phase noise and capability to operate at supply voltages ranging from 3.3V to 5V. A completely integrated implementation is a challenge in the 0.5 μ m technology. To provide the dc control voltage for VCO, a dead zone free phase frequency detector (PFD) and a compensated charge pump (CP) with a third order loop filter (LF) have been designed to achieve a fast lock time with minimum jitter. A Dual-Modulus Divider (DMD) is used to frequency scale the feedback VCO frequency. The dc frequency control value is maintained by the output of a phase/frequency detector, which serves as an "error amplifier" [1]. PFD provides

the phase difference between the input reference signal and the feedback signal from the VCO. Charge pump in turn plays a crucial role in transforming the phase/frequency pulsating output of the PFD to the corresponding charging and discharging currents for the LF. The smooth filtered voltage output of the LF is made available to the VCO as a control voltage. The Dual modulus divider is used because higher reference frequency is more desirable for increasing the overall system bandwidth and hence the speed with which PLL gets locked. Also with a higher reference frequency, the division ratio decreases and hence the divider noise decreases [2]. An overall block diagram of the whole design is shown in Fig. 1.

Figure 1. Overall Architecture of Frequency Synthesizer

2. Circuit Description

Design considerations for compactness, low power, high linearity, fast settling time and good noise characteristics were infused in the design cycle from the beginning and this resulted in a chip which met all the desired specifications. A discussion of each of the frequency synthesizer components and the corresponding key design deliberations are provided below.

2.1 Phase Frequency Detector, Charge Pump & Loop Filter

Figure 2. Dead-Zone Free PFD

The main criterion in designing PFD and Charge Pump is to minimize the spurious frequency components and the phase noise. The factors responsible for increasing phase noise and spurious tones are: dead-zones in PFD/charge pump

combinations and the charge pump charging-discharging current mismatch. To avoid a dead zone region, which usually occur, when the reference and the VCO feedback signal are near their lock state, an appropriate delayed reset was designed to minimize the dead zone. Fig. 2 presents the block diagram of PFD containing the delay and reset elements. Typical power consumption of PFD is 352.36 pW.

The charge pump (CP) is designed to stabilize the spurious fluctuation of the currents and the switching time to minimize the spurs in the VCO input. The design ensures provision of similar currents of approx. 100 μ A through both charge pump switches. This is achieved by using current mirrors for both the charging and discharging currents. The bias circuitry maintains a continuous current and provides both temperature immunity and equalization. The charge pump schematic is shown in Fig. 3a. The CP power consumption is less than 633 mW.

Figure 3. Schematics for (a) Charge Pump, (b) Loop filter

A third order loop filter (LF), having 3 poles and 1 zero, has been designed to provide a low noise dc input voltage for the VCO. Several reasons for choosing the third order LF include less spurious noise and a decrease in the size of the largest required capacitor. The size of the capacitors is critical as they occupy a large die area (see the complete chip layout, Fig. 12). A lower capacitance value will decrease the chip size markedly, but good integration of PFD/CP output demands a larger one. The on-chip layout is a compromise of both these conflicting demands. The third-order LF schematic is shown in Fig. 3b.

2.2 Dual-Modulus 32/33 Divider (DMD):

Realization of a high-speed fractional divider in a mixed mode environment should be such that it contributes minimum noise to sensitive analog circuits such as VCO, which share the same substrate with noisy circuits. This also ultimately effects the quality of the synthesized output signal. Current-mode logic (CML) is preferred to static CMOS logic for implementing the DMD. CML uses a constant current source, which causes lower digital noise generation. Differential signals are used at both input and output, which reduces the coupling noise from the supply line and substrate because the inherent differential architecture rejects the common-mode power supply and the substrate noise. However, logic swing is somewhat constrained, and the transistors are not operated in deep cutoff or saturation, resulting in an improved operating speed of the circuit.

Another key issue is reducing the power consumption for a given frequency range. Most power consumption in a fractional divider occurs in the front-end synchronous divider because it is the part of the circuit operating at the maximum frequency of the input

VCO signal. In our design, tail currents for synchronous and asynchronous dividers were kept different from each other because the asynchronous divider, working at a lower frequency, is able to give the desired performance at much lower current. For designing various logic gates, the same CML topology is used.

Figure 4. 32/33 Dual-Modulus Divider

The block diagram of the dual modulus divider is shown in Fig. 4. It consists of a “2/3 synchronous divider” and a “by-16 asynchronous divider”. The divide ratio of 2/3 synchronous divider is controlled by the mode control signal (MC) and by-16 asynchronous divider output. Divide by 3 operation is executed only one time over every cycle of 1/32. Gates G1 - G2 and flip-flops F1 - F2 construct the 2/3 synchronous divider.

2.2.1 D-Flip flop in CML Topology

Each D flip-flop of DMD has been designed using CML topology to be edge triggered and differentially clocked. The circuit diagram of the basic D-latch used for constructing master slave edge triggered D flip-flop is shown in Fig. 5. The top PMOS transistors are biased in the triode region using a replica biasing circuit. The W/L ratio of M1 and M2 is designed to get sufficient logic swing while optimizing power consumption. Transistors M7 and M8, which are connected to the clock, are kept at medium size to ensure that they switch rapidly even for low input swing of the differential clock. The bottom transistor M9 is for implementing a current source and is somewhat larger. Maximum current through transistor M9 is around 20mA. Transistors M3, M4, M5 and M6 form switching pairs and hence are kept at minimum W/L permitted by the technology. The W/L ratio of PMOS transistors in D-latches used for asynchronous divider is at half of that in the synchronous divider to reduce current and the corresponding power consumption. The tail current of the synchronous divider is approx. 114 μ A and that of asynchronous divider is approx. 46 μ A. Typical clock swing required is around 1V_{p-p}. Total Power Consumption is 6.966 mW.

Figure 5. D-latch implemented in CML Topology

The circuit diagram for four input OR gate is shown in Fig. 6 along with a common structure which can either be used as an AND/OR gate by appropriate selection of input connections.

Figure 6. (a) four input OR gate in CML topology
(b) Common structure for 2 input AND/OR gate

2.3 Voltage Controlled Oscillator

A negative g_m cross-coupled, fully differential, LC tuned, single control, voltage controlled oscillator (VCO) was implemented as shown in Fig. 7. The VCO also has an integrated source follower driver stage to improve its driving capability to interface with other on-chip circuits as well as external loads.

Figure 7. Integrated LC Voltage Controlled Oscillator

The on-chip 3-metal stacked inductor with a minimum Q of 4.66 was designed using the ASITIC CAD tool [6]. The inductor resonance frequency is greater than 3.3 GHz. In an iterative design process, the complete π model, including the series and shunt parasitic elements were extracted from the CAD tool. Due to the presence of only 3 metals in the technology, a patterned ground shield (PGS) structure was created using the poly layer.

The passive tank circuit was designed for minimum bias current as well as to accommodate for the parasitic elements of the on-chip inductor and capacitor. This technique gave simulated results, which match the layout results very closely. The bias current was chosen to be 7mA based on the frequency characteristics of the equivalent tank circuit.

The variable varactors are realized using PMOS technology. An inter-digitating layout is used to minimize the stray resistance

and hence increasing the Q of the varactor. For layout of large size MOS transistors, a fingered multiplicity structure was used as it minimizes the junction capacitance and speeds up charge recovery while allowing for a compact physical realization.

Figure 8. VCO Voltage-Frequency Characteristics

The resulting VCO has nice linear voltage-frequency characteristics in the GSM frequency domain. It can operate at supply voltage ranging from 3.3V to 5V, with corresponding power dissipation in the range of 16.5 mW to 56.5mW. The peak-to-peak output voltage swing is a function of this supply voltage.

3. Simulation Results

Initial simulation of the DMD was carried out at 1GHz input frequency. The waveforms at the output of 2/3 Prescaler and 32/33 Dual-Modulus Divider are presented. The Modulus Control (MC) is high for the period of 100ns. When MC is high, one extra clock cycle is swallowed per 32 input clock cycles.

Figure 9. Dual Modulus Divider: Simulation Results

The VCO has phase noise characteristics of less than -117 dBc/Hz at 100 kHz offset from the carrier frequency close to 900 MHz, see Fig 10a. The frequency synthesizer output signal is very close to an ideal sine wave (Fig. 10b).

Figure 10. VCO Simulations (a) Phase Noise Characteristics (b) Transient output at 900 MHz

4. Fractional Division using Accumulator

The primary motive in using a fractional-N architecture is to improve the phase noise characteristics. In this proposed scheme, frequency resolution is a fraction of the reference frequency F_{ref} . Maintaining a higher F_{ref} , the overall division ratio N can be kept small. Further, increasing F_{ref} makes it possible to improve the switching speed as well as increasing the loop bandwidth. The scheme for fractional division is shown in Fig. 11.

Figure 11. Channel Selection using Phase Accumulator

The Accumulator changes the divisor N to $N+1$ by commanding mode control signal to dual modulus divider. The timing of the accumulator is clocked by the VCO signal (after division by N). Each time the accumulator overflows the carry out goes from low to high and the division ratio is commanded to increment to $N+1$. In the locked state, the VCO output frequency is given by

$$F_{vco} = (N + K/F) F_{ref}$$

where K is the programmable value that is equal to the number of times the dual modulus divider divides by $N+1$ in a full fractional divide cycle and F is the value that determines the number of reference cycles that are in each full fractional divide cycle. F is equal to the size of the accumulator, e.g.,

Selecting frequency synthesis parameter for GSM mobile transmit band (i.e., 890-915MHz). Required channel spacing (frequency resolution) for GSM is 200 kHz. F_{ref} is kept at $890/32 = 27.8$ MHz. For F_{ref}/F to equal desired resolution of 200kHz, F is selected to be 139 and realized by an 8-bit accumulator with feedback and overflow settings at 139.

The complete Frequency Synthesizer Architecture is presented in Fig. 12.

Figure 12. Complete Frequency Synthesizer Layout

5. References

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