

Precise RSSI with High Process Variation Tolerance

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Abstract— A receiving signal strength indicator (RSSI) built with transconductance amplifiers is presented. The RSSI achieves high tolerance to process variations by utilizing the unique nature of branch currents in a transconductance amplifier. These branch currents are used to implement a current-mode rectifier and amplitude clipping circuit that are tolerant of process variations. An on-chip offset control loop permits the entire RSSI to be realized with only one external component. In 0.18 μm CMOS with a 1.8V supply, the RSSI draws 2.5mA and provides 80dB of offset suppression and more than 70dB of log-linear range with less than $\pm 2\text{dB}$ error due to process variation.

I. INTRODUCTION

In wireless communication, signal strength can vary over several orders of magnitude. To ease the dynamic range requirements of the analog-to-digital converter (ADC) in the receiving channel, the gain of the receiving path should be adjustable to provide a stable, large-swing output over a span of input signal magnitudes. A receiving signal strength indicator (RSSI) is used extensively in wireless transceivers [1,2] to provide the information necessary to adjust receiver gain. The ability for RSSI circuits to monitor the presence of signals is also useful in power management applications.

To cover several orders of signal magnitude, the RSSI is generally realized in a logarithmic-linear form. A successive-detection architecture has commonly been used [3-5] because it is more accurate than the alternative structures based on PN-junctions. Fig. 1 shows the general block diagram of a successive-detection RSSI. This approach is based on the linear approximation of the logarithmic transfer function. The detection range of this RSSI is determined by the total gain of the limiting amplifier chain. The accuracy is determined by the gain of each stage and is improved by smaller gain per stage. In practice, 12dB per stage provides sufficient precision.

Traditional RSSI circuits suffer from intolerance to process variations, requiring hardware or software for calibration and compensation. Successive detection

rectifiers commonly use unbalanced differential pairs [4] or specially biased input pairs [3,5]. The transfer functions of these approaches are strongly affected by device parameters that fluctuate with process variations. The limiting amplifier used in RSSI circuits must provide enough bandwidth for IF signals. The MOS-driving-MOS structure [3-5] is a wide bandwidth, low power, open loop design for limiting amplifiers, wherein gains are defined by the transconductance, g_m , ratios of the loading and driving MOSFETs. The voltage clipping point is also related to g_m . However, these values fluctuate undesirably with process variations.

To eliminate the need for complicated and costly calibration, it is desirable to minimize RSSI errors due to process variations. This paper describes a new, wide bandwidth, process-tolerant RSSI circuit that is based on a transconductance amplifier with resistive source degeneration. A method is proposed to perform current-mode rectification and amplitude clipping utilizing special features of the branch currents in transconductance amplifiers. Current-mode operation permits independence from transistor process variations, and a resistor-value-tracking bias current suppresses errors due to process variations in on-chip resistors.

The transconductance amplifier with constant gain is described in section 2 along with its novel use in a current-mode rectifier and amplitude clipping circuit. Based on this transconductance amplifier, an RSSI structure and circuit are described in section 3. Finally, the results and conclusions are given in sections 4 and 5, respectively.

II. CONSTANT GAIN TRANSCONDUCTANCE AMPLIFIER

A transconductance amplifier with a stable gain has been designed. As shown in Fig. 2, it utilizes resistive source degeneration to improve linearity [6]. The unique feature of its branch current facilitates current-mode rectification and amplitude clipping functions that can be incorporated into a process tolerant RSSI.

A. Process Variation Tolerant Gain

In Fig. 2, V_{bp1} , V_{bp2} , V_{bn1} and V_{bn2} are bias voltages of the transconductance amplifier. Because its output is differential, a common mode feedback (CMFB) block is used to set the proper common mode voltage at the output. the input PMOS V_{GS} is constant because its drain current is fixed. Thus, the input voltage difference is exactly transferred onto R_1 , and the voltage gain, A , is defined by

$$A = \frac{K \cdot R_2}{R_1} \quad (1)$$

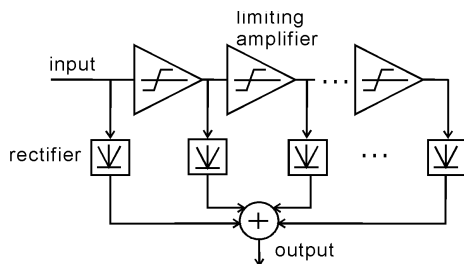


Figure 1. Typical architecture of the successive detection RSSI.

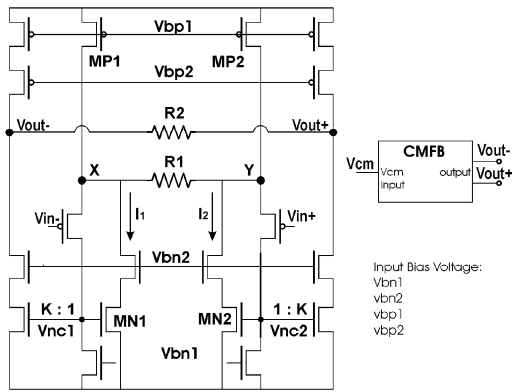


Figure 2. Transconductance amplifier with process variation tolerant gain.

where K is the current scaling ratio of two current mirrors involving MN1 or MN2, and $R1$ and $R2$ are shown in Fig. 2. Because $R1$ and $R2$ are built with the same type of on-chip resistors and placed very close to each other, their matching is very good and nearly independent of process variation. Thus, the voltage gain of the circuit in Fig. 2 is very stable against process variation.

The finite output resistance of the MOSFET in parallel with $R1$ & $R2$ will affect the gain precision and stability across process variations. Several measures have been taken to suppress this effect. The output branches use a cascode structure to increase their output resistance and minimize their effect on $R2$. To minimize the effect of MOSFET output resistance on $R1$, the NMOS branch at nodes X and Y is cascoded. For the PMOS branch at nodes X and Y, a single transistor (MP1 or MP2) with long gate length is used to avoid limiting the voltage swing with a 1.8V supply.

B. Method for Rectification and Amplitude Clipping

The transconductance amplifier does not directly provide the amplitude clipping and rectification functions that are necessary for a successive detection RSSI. However, the characteristics of its branch current, I_1 and I_2 in Fig. 2, can be manipulated with additional circuitry to realize these functions in current mode. Current-mode rectification minimizes the effects of transistor parameter variation and achieves high process tolerance and precision. Also, the current amplitude clipping point is completely determined by the bias current, and it is independent of the process variations in transistors within the main RSSI circuit (see details in section 3).

Fig. 3 shows the response of I_1 and I_2 to three input sinusoid waves of different magnitudes. Notice that, beyond a certain input magnitude, the negative amplitude of both currents will be clipped to zero. The absolute value of the negative amplitude actually is the balanced DC current of these branches, which can be very well controlled by the bias circuit. In contrast, the positive

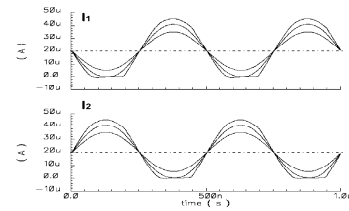


Figure 3. Branch current for input swings below, at, and above the limiting point.

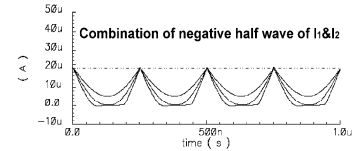


Figure 4. Response of the rectification and amplitude clipping to input sinusoid with swings below, at, and above the limiting point, created by combining the negative half wave of branch currents in Fig. 3.

amplitude of I_1 and I_2 continues to increase because MP1 (or MP2) will go into the triode region and continue to supply more current as the input increases further, but the response is no longer linear. Thus, the response of I_1 and I_2 provide the desired amplitude clipping function for only the negative half-waveform.

To realize full-wave rectification and amplitude clipping, a current that consists of only the negative half waves of I_1 and I_2 can be produced as a response to the sinusoid inputs, as shown in Fig. 4. This waveform is a typical output of the rectifier in a successive detection RSSI for a sinusoidal input. The absolute value of the negative clipping amplitude is determined by the bias current.

III. RSSI BASED ON TRANSCONDUCTANCE AMPLIFIER

Fig. 5 shows the block diagram of an RSSI constructed around six cascaded gain stages. The gain stages are composed of transconductance amplifiers and dedicated circuits to realize current-mode amplitude clipping and rectification (by generating the waveform as shown in Fig. 4). The gain of the transconductance amplifier in each stage is set to 12dB, so the total gain of the RSSI is 72dB. Two gain stage variations, one with DC offset control and one without, are utilized in this design. An on-chip resistor is used to convert the RSSI output current to a voltage (V_{out}). An off-chip capacitor in parallel with the on-chip resistor filters out the AC components at V_{out} .

A. Common Bias Generator

The common bias generator in Fig. 5 biases all of the RSSI circuit blocks, including the transconductance amplifier. As described above, the current-mode amplitude clipping point is completely determined by the bias current. The output of the RSSI is a voltage obtained by applying the rectified currents of the gain stages to the on-chip resistor. To suppress the output error due to resistor

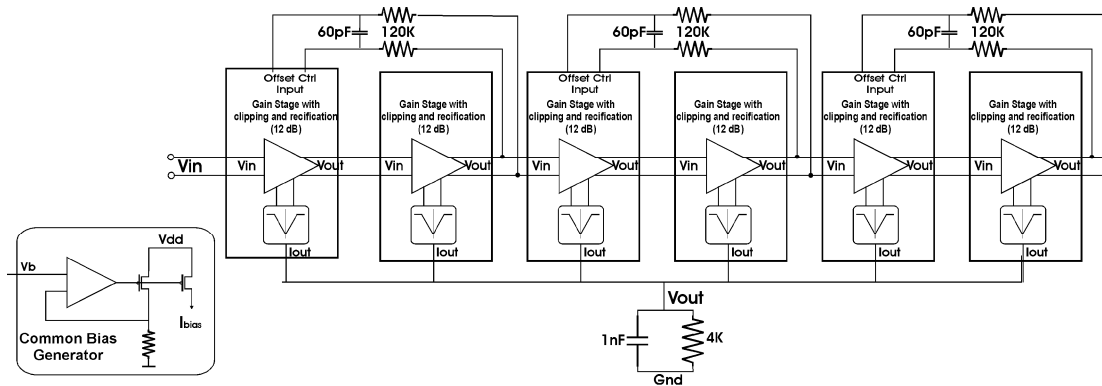


Figure 5. Block diagram of the new RSSI.

process variations, the bias circuit generates bias currents that track the on-chip resistor value. Fortunately, a transconductance amplifier transforms its input voltage to a current through another on-chip resistor (R_1 in Fig. 2). Thus the bias current also ensures the input referred transfer function is tolerant of process variations.

B. Gain stage design

The schematic for each RSSI gain stage is shown in Fig. 6. The baseline circuit consists of a transconductance amplifier (top right) and a circuit to implement current-mode amplitude clipping and rectification (bottom right). A second type of gain stage includes the circuit enclosed by a dotted line to provide an input for offset control. Fig. 5 shows how these two circuit variations come together to form the overall RSSI.

The transconductance amplifier shown in Fig. 6 is the same as in Fig. 2. By setting $K=2$ and $R_2=2R_1$ in Equation(1), the transconductance amplifier gain is designed to be 12dB ($4\times$). The bias current is selected so that the negative swing of I_1 and I_2 (Fig. 3) are clipped to zero with an input voltage reaching clipping point. This voltage reflects the voltage drop on R_1 because the V_{GS} 's of the input PMOS are fixed. Because the bias current tracks resistor variations, this input referred clipping voltage is independent of process variation.

The circuit beneath the transconductance amplifier in Fig. 6 utilizes half wave clipping of I_1 and I_2 to achieve full waveform rectification and amplitude clipping. The circuit can be split into left and right halves. Each half first mirrors I_1 and I_2 and then realizes the half-waveform rectified current in MP3 or MP4. Finally, these two half-waveform rectified currents are summed to form I_{out} . Fig. 7 shows the resulting waveform for sinusoidal input signals of three different amplitudes. In these current-mode manipulations, transistor matching plays a key role in accuracy because the currents are mirrored several times. Careful layout can guarantee good size matching and protect against process variation. Thus this current-mode operation is nearly independent of transistor process variations.

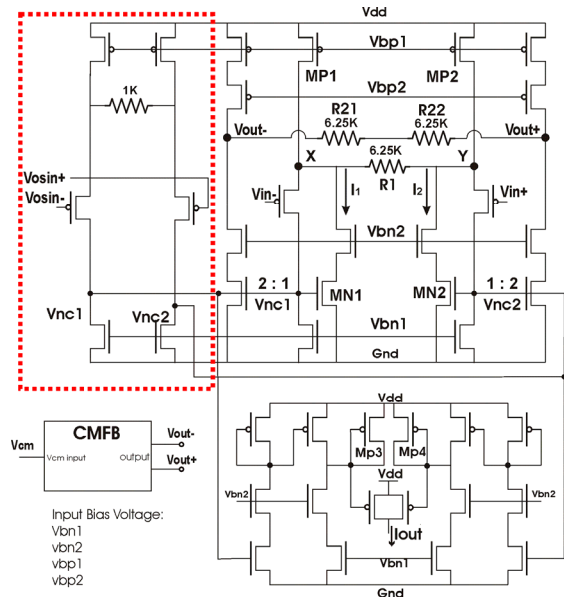


Figure 6. Circuit for gain stage, circuit in enclosed area is used for chain offset control and only appears in gain stage with offset control.

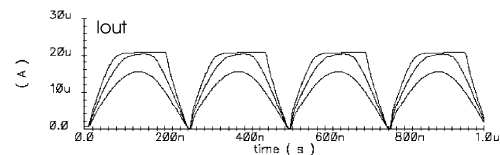


Figure 7. Waveform of I_{out} responding to input swing of below/at/above the limiting point.

C. Gain Stage Chain DC Offset Control

Due to the large gain of the amplifier chain, the DC offset of each amplifier in the chain becomes a major liability. Even a minuscule input referred offset voltage would saturate the chain's internal nodes and limit the detection floor. Thus DC offset control is necessary. In [3], a single low pass filter loop was adopted to suppress the DC offset. Due to the large gain in the chain, a very large off-chip capacitor was necessary to provide a sufficiently low cutoff frequency. In contrast, the RSSI in Fig. 5 breaks the feedback into three loops, and the required capacitors in each loop are small enough to be realized on-

chip. The feedback loop could be broken into more sections, but the input referred residue offset would increase with adverse impact on RSSI resolution. Three feedback loops significantly improve DC offset control with negligible effect on resolution. Fig. 8 plots the simulated AC response of the whole chain and shows an 80dB DC offset suppression is achieved. The offset canceling feedback loops are integrated with the transconductance amplifier through an auxiliary input shown within a dotted region in Fig. 6.

IV. RESULTS

The RSSI circuit of Fig. 5 was implemented using the IBM 0.18μm CMOS process. The fabricated circuit, shown in Fig. 9, occupies 0.4mm x 0.5mm and draws

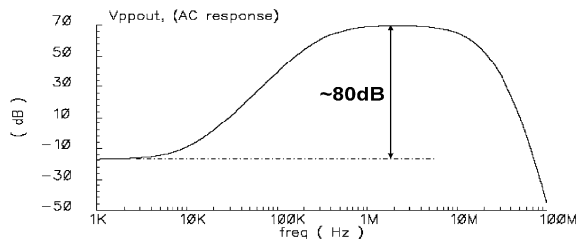


Figure 8. Frequency response of the gain chain.

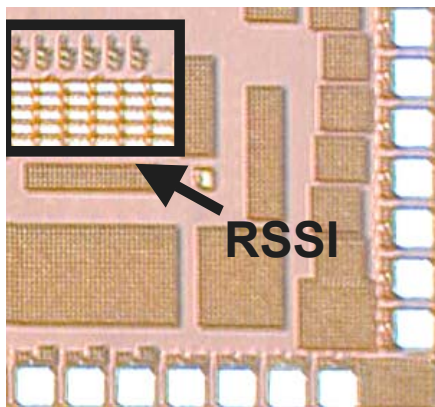


Figure 9. Chip photograph of the RSSI circuit

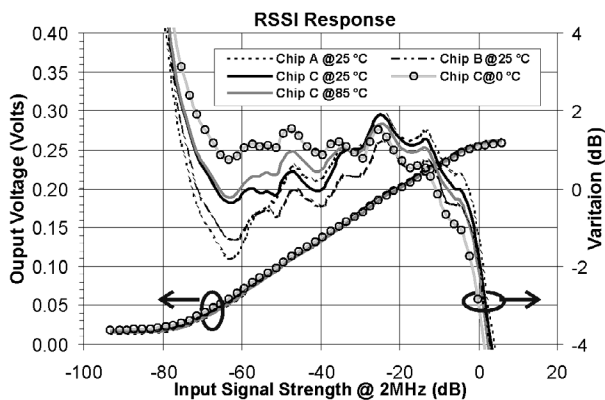


Figure 10. Measured RSSI response and error plotting

TABLE I. SUMMARY OF RSSI PERFORMANCE

Technology	IBM 0.18μm CMOS,
Area	0.4mm X 0.5mm
Power	2.5mA
Log-linear range	70dB
Process variation error	+/- 2dB

2.5mA from a 1.8V supply. Fig. 10 shows the RSSI response. With a 2MHz input, it provides more than 70dB of log-linear range. To verify process tolerance, the transfer function was measured on three randomly selected chips and one chip was measured at three different temperatures. The overlap of the responses in Fig. 10 illustrates the output is very stable with process variation. Fig. 10 also plots the variation in the five measurements shown on the right Y-axis. Table 1 summarizes the performance of the RSSI circuit.

V. CONCLUSION

A new approach for implementing a precise, process tolerant receiving signal strength indicator (RSSI) was presented. It utilizes the unique nature of branch currents in a transconductance amplifier to realize a nearly ideal, current-mode rectifier and amplitude clipping circuits that suppress process variations. No calibration is required for this RSSI because it compensates for process variation internally. In 0.18μm CMOS with a 1.8V supply, the RSSI draws 2.5mA and provides more than 70dB of log-linear range. Furthermore, the on-chip offset suppression loop minimizes the necessary external components to only one, which is important for reliability and low cost.

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