

Post-CMOS electrode formation and isolation for on-chip temperature-controlled electrochemical sensors

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A low-cost post-CMOS fabrication process enabling the formation of thermally controlled and isolated microelectrode array sites suitable for biomimetic and bioelectronic protein attachment on existing CMOS circuitry has been developed and implemented in the fabrication of an electrochemical array system for biosensing applications.

Introduction: Recent advances in protein-based biomimetic and bio-electronic interfaces on metal electrodes [1] generate an opportunity to form integrated electrochemical sensors that can simultaneously measure multiple analytes for a wide range of molecular analysis applications. The proteins within these biointerfaces show optimal sensitivity at different temperatures, typically between room temperature and 100°C. These novel biointerfaces can best be realised as biosensors using technologies associated with integrated microsystems, which offer the advantages of repeatability, scalability, low cost, small size, and high density capability. To date, various forms of three-electrode electrochemical systems have been integrated on silicon chip surfaces [2, 3], but none offers the thermal control capability needed to maximise protein reactivity. The fabrication and characterisation of on-chip structures for thermal control have been widely reported, particularly for use in micro-hotplate gas sensors. However, systems combining electrochemistry and thermal control have not been reported. This Letter introduces a low-cost post-CMOS fabrication process enabling the formation of thermally controlled and isolated microelectrode array sites suitable for protein attachment and electrochemical interrogation using embedded CMOS circuitry [4].

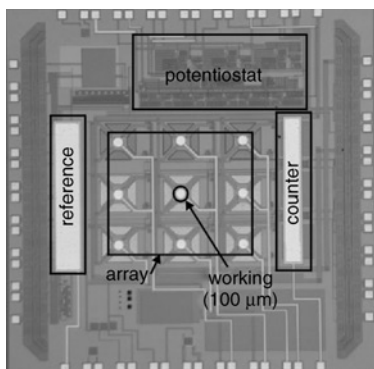


Fig. 1 Die photograph of 3 × 3 mm CMOS chip with 3 × 3 array of thermally isolated working electrode sites for electrochemical biosensors

Microelectrode array design: The fabricated microelectrode array system consists of nine biocompatible gold working electrode array sites, each thermally isolated and incorporating a resistive heating and sensing element, a gold counter electrode, and an Ag/AgCl/Nafion reference electrode [2]. To simplify post-fabrication processing and minimise the associated cost, this electrode array design utilises common CMOS process layers as masking layers, sacrificial layers, heating elements and interconnection of on-chip circuits to surface gold electrodes. The 3 × 3 mm base array chip, shown in Fig. 1, was fabricated in AMI Semiconductor's C5F/N 0.5 μm process, a planarised, non-silicided CMOS process supporting stacked contacts with three metal layers and two polysilicon layers, one of which is a high resistance layer, tolerant to 20 V. The common reference and counter electrodes are large rectangular stacks of CMOS metal layers exposed by an overglass opening. Each of the nine ~100 μm diameter working electrode sites consists of a serpentine polysilicon heating element beneath a 200 kΩ polysilicon sensing element and a circular stacked metal electrode that is also exposed through an overglass opening. Because the C5 N process is planarised and does not support oversized contacts or vias, no direct opening to the silicon substrate is available through the foundry process. Hence, surface-exposed CMOS metal stacks have been added around the working electrode sites to

serve as sacrificial layers, facilitating access to the substrate through vias and contacts in order to release the thermal isolation structures.

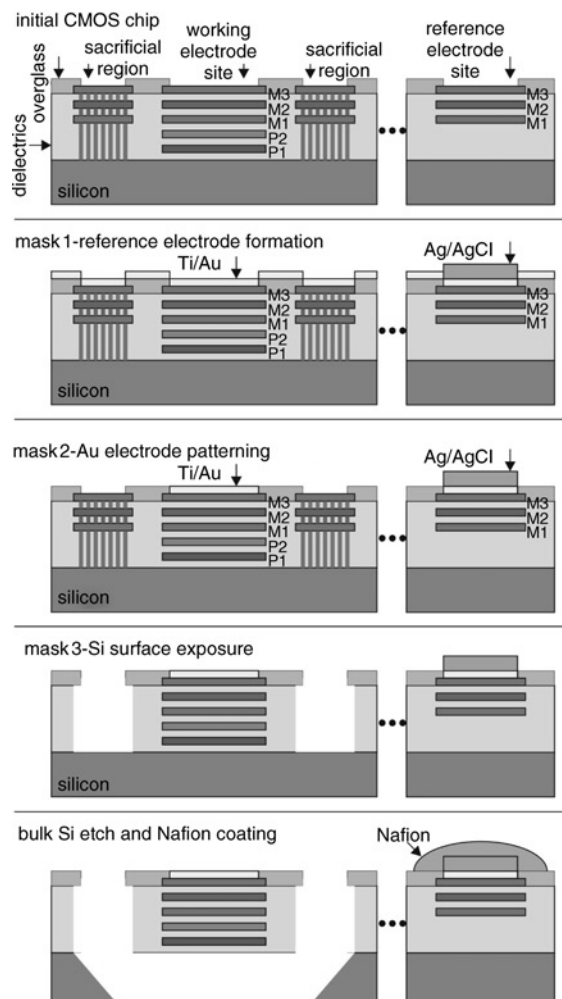


Fig. 2 Post-CMOS fabrication process flow for formation of surface electrode array with thermal control and isolation

Electrode formation and thermal isolation: A low-cost, highly repeatable, post-CMOS fabrication process has been developed to form biocompatible thermally isolated electrodes utilising thin-film metal deposition, photolithography and wet etching. The simple three-mask process, shown in Fig. 2, utilises microfiche masks [5], which can resolve down to 1 μm features using a 25× reduction ratio during mask generation and has the advantages of being both inexpensive and quickly produced. Initially, a 100 Å titanium adhesion layer and 100 nm gold layer are deposited using an AXXIS E-beam physical vapour deposition (PVD) system. A mask pattern is then applied to the surface using photolithography with microposit 1813 positive photoresist (PR) and a Suss MJB3 submicron mask aligner. E-beam evaporation is then used to deposit 100 nm of silver on the patterned surface, and the chip is soaked in acetone to form the Ag base for the reference electrode via lift-off. The chip is then coated with PR and patterned with the same mask before being placed in a 1 M FeCl₃ solution for 120 min at 30°C to form the Ag/AgCl reference electrode. After the PR is removed, the chip is placed in a desiccator for 24 h. Subsequently, the second mask is transferred, the gold is etched in gold etchant type A (KI) for 30 s, and the titanium is etched in buffered hydrofluoric acid (BHF 1:5) for 1 s with the silicon nitride overglass preventing the etching of oxides on the CMOS chip. Next, the chip is patterned with the third mask, which allows access to the sacrificial CMOS layers while preventing the undercut of the newly patterned Ti/Au electrodes. Three subsequent etches in BHF (removes oxide and TiN layers) for 5 min and aluminium Type I etchant (phosphoric + acetic + nitric acid + water 16:1:1:2) at 50°C with agitation for 1 min followed by a final 5 min BHF etch removes the three TiN/AlCu/TiN CMOS metal layers and the intermetal dielectrics, providing surface access to the silicon substrate. Finally, the bulk silicon beneath the working electrodes

is anisotropically etched for 90 min with a 10% tetramethylammonium hydroxide (TMAH): 0.5% ammonium persulphate: 1% silicon solution at 80°C while agitated, undercutting and releasing the working electrode array thermal isolation island structures. Areas outside the exposed silicon are masked by overglass and surface metal layers. Ammonium persulphate and dissolved silicon in the solution prevent the etching of the bond pads. Nafion is then applied over the reference electrode and the final chip is again placed in a desiccator for 24 h.

Results: The final temperature controlled electrochemical biosensor array chip contains a reference electrode, a counter electrode, and nine thermally isolated working electrode array sites. Each working electrode provides 200 k Ω sensing resistors and a polysilicon heating resistor with values ranging from 195 Ω to 2.6 k Ω . The final chip was cemented and wirebonded to a copper etched board, and the wirebonds and exposed copper, except for the solder pads, were covered with epoxy to prevent conduction in solution. The sensor array was immersed in potassium ferricyanide and various cyclic voltammograms were generated using an Omni-101 potentiostat, confirming electrochemical functionality. The serpentine polysilicon resistors, which experience Joule heating, were found to be functional, glowing red with increasing intensity, generating upwards of 400°C (well over temperatures of interest for protein-based biosensors) as the control voltage was increased, and the resistance of the sense resistors was observed to increase accordingly, as shown in Fig. 3.

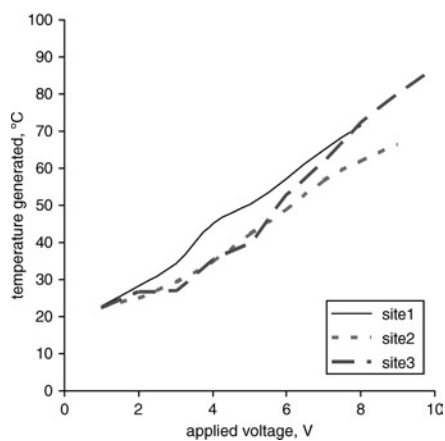


Fig. 3 Temperature generated against applied voltage for thermally isolated temperature controlled electrodes

Conclusions: A low-cost post-CMOS fabrication process enabling the formation of thermally controlled and isolated microelectrode array sites suitable for biomimetic and bioelectronic protein attachment on existing CMOS circuitry has been developed. The simple mask set and exclusive use of wet etching drastically reduce the cost of the system while the small electrode size increases sensitivity. By implementing this process, a thermally controlled and isolated 3 × 3 gold working electrode array and common counter and reference electrodes have been fabricated on a CMOS chip, packaged and tested in an electrochemical cell. These features make the system an ideal platform for high volume, high sensitivity, low-cost integrated bioelectrochemical sensor applications.

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