Impedance-to-Digital Converter for Sensor Array Microsystems

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Abstract—Many emerging micro/nano sensor interfaces suitable for microsystem integration produce a change of impedance that must be monitored over a broad frequency range. This paper introduces a mixed-signal integrated circuit that can extract and digitize the real and imaginary components of a sensor’s impedance response. The ultra compact size of this circuit enables each element in a multi-channel sensor array microsystem to have its own individual readout channel, permitting simultaneous readout and digitization of a high density sensor array. The circuit was fabricated in 0.5µm CMOS and occupies only 0.045mm² per cell. With a 3.3V supply, each cell consumes only 5.2µW at a typical 200kHz sampling frequency. For a 3mm by 3mm die, this circuit can be instantiated well over 100 times, which is sufficient for the needs of many anticipated sensor array microsystems.

I. INTRODUCTION

Arising from the growth of nanotechnologies, many new and promising sensor interfaces have been introduced in recent years, particularly for biological and chemical sensing. Many of these produce electrical responses that make them well suited for microsystem platforms. For example, electronic biosensors are considered among the most promising technologies for next generation high-performance bioanalysis systems for DNA testing, drug screening, security enhancement, and related applications [1]. Many of these new interfaces elicit a response that is measured by a change of impedance over a range of stimulus frequencies, which is referred to as impedance spectroscopy (IS). IS techniques are wildly used to monitor the activities of membrane protein biosensors [2, 3], gas sensors [4] humidity sensors [5] and DNA sensors [6], and they can also be used to characterize intrinsic electrical properties of many materials or interfaces.

Due in part to the progress being made in CMOS compatible fabrication of microelectrodes [1], there is a trend to build sensor array microsystems that deposit miniaturized sensor array on the surface of silicon chips and interrogate these sensor elements with on-chip electronics [6, 7]. Traditionally, IS measurements require complex and bulky electronics or utilize digital signal processing algorithms that require extensive computer hardware. To support chip-scale microsystem applications, a very hardware efficient and low power solution is needed that combines accurate, low noise impedance measurement circuits with electronics capable of extracting real and imaginary signal components to circumvent the heavy signal processing load involved in parallel impedance extraction of a sensor array [7]. Some impedance measurement systems have built for miniaturized biomedical and biochemical systems [8-10], but they either lack the integration of measurement, extraction, and digitization functions or they fail to support multi-channel array-based systems.

In this paper, a compact, high-sensitivity lock-in impedance-to-digital converter (IDC) circuit for sensor array microsystems is presented. The lock-in IDC cell is based on a delta-sigma structure and can be instantiated for each sensor element to enable massively parallel interrogation, including analog domain impedance extraction and local digitization. Its low power consumption extends the battery-life for portable applications and protects on-chip sensors from overheating. It also provides high sensitivity to read the very weak responses characteristic of miniaturized sensor elements. Compared to our prior work [11], the new circuit presented here adds DC impedance readout capability and implements design modifications that reduce power and area and thus improve its utility in array-based microsystems.

II. IMPEDANCE SPECTROSCOPY MEASUREMENT METHODS

In the impedance spectroscopy measurement technique, a stimulus with known frequency content is applied to a test source, such as a sensor interface. The resulting output response contains a phase and/or amplitude shift, algebraically related to real and imaginary components impedance components, which are extracted using either an analog circuit or the Fast Fourier Transform (FFT) algorithm [12]. The FFT algorithm utilizes a broadband stimulus, such as a pulse, and computes the result at all frequency points simultaneously, producing an impedance spectrum. The composite signal source and the computationally intensive Fourier transform require FFT-based IS instruments to use personal computer or a digital signal processor (DSP) with extensive computational resources [13]. Although some works have been done to realize the FFT with analog circuits [14], it does not appear to be practical approach for microsystem implementations due to poor multiplier linearity and accuracy and demands for preprocessing/pre-storing of the input data set. Furthermore, the hardware and power demands of FFT-based systems are compounded in multi-channel sensor array applications. Alternatively, the frequency response analyzer (FRA) based method can be realized with compact analog circuits. The FRA method processes the response of one frequency point at a time. It is a pure technique that gives rise to very stable, repeatable measurements and is able to minimize the effects of noise and distortion [12].
Theory of Operation

To describe FRA method and the operation of the lock-in IDC, consider a sensor interface stimulated by a sinusoidal voltage, \( \sin(\omega t) \), and producing a current response \( I_x \) such that

\[
I_x = A \sin(\omega t + \theta) = \sin(\omega t) + b \cos(\omega t)
\]

(1)

where \( A \) and \( \theta \) represent the amplitude and phase, of the sensor’s impedance, respectively. Here \( a = A \cos(\theta) \) is the real portion and \( b = A \sin(\theta) \) is the imaginary portion of the sensor’s admittance (the reciprocal of impedance). The values of \( a \) and \( b \) over a wide frequency range are sufficient to fully describe the sensor’s impedance information.

To extract these values, a multiplying integrator was designed for the lock-in IDC. As shown in Fig. 1, the multiplier is driven by a square wave, \( \varphi(t) \). When control signal \( S \) in Fig. 1 is set to 0, \( \varphi(t) \) is in phase with \( \sin(\omega t) \) and described by

\[
\varphi(t) = \text{sgn}(\sin(\omega t)) = \begin{cases} 1, & nT < \pi \leq nT + T/2 \\ -1, & nT + T/2 < \pi < (n+1)T \end{cases}
\]

(2)

where \( T \) is the period of the stimulus and \( n \) is any integer. If (1) is multiplied by (2) and integrated over \( N \) continuous stimulus cycles, then the integrator’s output is given by

\[
\sum_{i=0}^{N-1} \int_T^{(i+1)T} \varphi(t) \cdot I_x dt = \int_T^{(i+1)T} I_x dt - \int_T^{(i+1/2)T} I_x dt
\]

\[= \frac{2T}{\pi} \cdot N \cdot A \cos(\theta)
\]

(3)

Notice that the integration result is proportional to the real portion of the sensor’s admittance, \( a \) in (1). Similarly, if the square wave \( \varphi(t) \) is in phase with \( \cos(\omega t) \) (when \( S=1 \)), its function is given by

\[
\varphi(t) = \text{sgn}(\cos(\omega t)) = \begin{cases} -1, & nT + T/4 < \pi < (nT + 4T)/3 \\ 1, & \text{else} \end{cases}
\]

(4)

and the result of the operations in (3) give

\[
\int_0^T I_x \cdot \varphi(t) dt = \frac{2T}{\pi} \cdot N \cdot A \sin(\theta)
\]

(5)

which shows that the result is proportional to the imaginary portion of the sensor’s admittance, \( b \) in (1). Thus, with a multiplier, an integrator, and two reference square-waves, impedance extraction function can be realized.

IDC Circuit Implementation

To implement the FRA functionality described above along with digitization of the resulting admittance value, the lock-in IDC structure shown in Fig. 1 was developed. It includes an analog multiplying integrator stage to realize impedance extraction via the FRA method and a comparator, a flip-flop, and a bidirectional counter for digitization. Without the switches controlled by \( \varphi \), the structure is similar to a traditional delta-sigma ADC, where the comparator is a 1-bit ADC and the reference currents are a 1-bit DAC. This structure was selected as the baseline for the IDC because it uniquely includes the integrating function required for impedance extraction and permits sufficient accuracy in a compact size with no external components required.

The first stage of the lock-in IDC is a multiplying integrator stage that based on our previous work [11], shares resources to realize both the multiplication and integration functions in Fig. 1. The multiplying integrator changes its polarity according to value of the square wave \( \varphi \).

To simplify analysis, assume that \( \varphi \) is in phase with \( \sin(\omega t) \) and that at all of \( \varphi \)’s transition edges both comparator results, \( D \) and \( D^* \), are low. If not, the multiplexing switches controlled by \( \varphi \) force \( D \) and \( D^* \) to exchange the polarity of charge injection through reference current \( I_{\text{ref1}} \) or \( I_{\text{ref2}} \). From time 0 to T/2, \( \varphi \) is high and the counter is counting up. Just before \( \varphi \)’s edge at time T/2, according to the change conservation theory, at the input node, we have

\[
\int_0^{T/2} I_x dt = CV_{\text{res1}} + I_{\text{ref1}} T_0 \sum_{i=1}^{N} D_i - I_{\text{ref2}} T_0 \sum_{i=1}^{N} D_i
\]

(6)

where \( V_{\text{res1}} \) is the residue value at the integrator output, \( T_0 \) is the updating clock period, and \( N \) is the number of clock cycles from time 0 to T/2. From time T/2 to T, \( \varphi \) is low, the integrator capacitor is reversed, and the counter is set to down counting mode. This mode produces

\[
\int_{T/2}^{T} I_x dt = C(V_{\text{res1}} + V_{\text{res2}}) + I_{\text{ref1}} T_0 \sum_{i=N+1}^{2N} D_i - I_{\text{ref2}} T_0 \sum_{i=N+1}^{2N} D_i
\]

(7)
where \( V_{res2} \) is the integrator’s output voltage at time \( T \). Simplifying the equation with \( D^* = 1 - D \) and combining (6) and (7), the full cycle produces

\[
\int_0^T I_x dt = -CV_{res2} + (I_{ref1} + I_{ref2}) \cdot T_0 \cdot \left( \sum_{i=1}^N D_i - \sum_{n=1}^{2N} D_i \right)
\]

(8)

Thus, the real result is represented by the contents of the counter (the summations in (8)), provided the circuit parameters are chosen such that \( |CV_{res2}| < \frac{1}{2} \min(I_{ref1}T_0, I_{ref2}T_0) \), where the residue on the integrator can be treated as noise. If the IDC is operated for \( N \) consecutive stimulus cycles after initial reset, the residue term in (8) remains in the same range while the digital part is magnified by \( N \). Therefore, the error due to ignoring the residual will decrease with repeated cycles.

Following a similar analysis, it can be shown that the counter will contain the imaginary portion of admittance when \( \phi \) is in phase with \( \cos(\omega t) \). Thus, by setting \( \phi \) to be in or out of phase with the stimulus sinusoid, the IDC circuit can extract both portions of the full impedance utilizing the structure then inherently digitizes the result while sharing resources to minimize size and power. The bidirectional counter also serves as a shift register to simplify data retrieval.

IV. TEST RESULT

The lock-in IDC readout circuit was fabricated in 0.5\( \mu \)m CMOS process and is shown in Fig. 3. Each fully functional channel, including the multiplying integrator, the comparator and the counter/shifter, occupies only 100\( \mu \)m \( \times \) 450\( \mu \)m. For testing, a data acquisition card (DAQ E2530A) was used to generate the sinusoidal stimulus voltage, reference square wave, global clock and digital control signals and to record digital outputs from the lock-in IDC chip. The equivalent impedance circuit for biomimetic membrane sensor interface [3] was utilized to characterize the chip, as shown in Fig. 4.

To verify the impedance extraction capability of the lock-in IDC circuit, a sinusoidal voltage stimulus with frequency from 0.1 Hz to 100Hz was applied to the biosensor circuit model. Fig. 5 plots the results obtained from the digital output of the IDC along with the theoretical curve for the model impedance. The lock-in IDC tracks both real and imaginary components of the test impedance very well, with a maximum mismatch of 1% of the full scale response.

Fig. 5 demonstrates that the IDC tracks static impedance over frequency very well. To characterize how well the responds to a variable impedance, IDC chip was measured by changing the phase and amplitude of the stimulus input independently. With a fixed input amplitude and frequency, the relationship between the input signal phase and the imaginary result is theoretically a sine wave. Fig. 6 plots the normalized IDC response to an input with a constant

Fig. 2. Simplified lock-in impedance-to-digital converter structure. \( \phi \) is the reference square wave.

Fig. 3. Photograph of a 1.5\( \times \)1.5mm chip with two lock-in IDC channels.

Fig. 4. Test platform for the IDC chip with biosensor equivalent circuit model.
amplitude and frequency and variable phase. When fit to the expected sine wave, a Root Mean Square error of only 0.07 was obtained, demonstrating that the IDC tracks variable impedance very well. Although the results are not shown here, a similar test was performed using an input with fixed frequency and phase but variable amplitude. As expected, the real portion of the IDC results was found to increase linearly with the input signal amplitude from 0.1V to 1V. Operation of the IDC was verified over wide frequency range, 0.01-10kHz, suitable for many sensors interfaces.

V. CONCLUSION
An integrated circuit capable of performing impedance spectroscopy measurements on an array of sensor interfaces has been described. Based on the delta-sigma ADC architecture, the new impedance-to-digital converter utilizes mixed-mode signal processing to extract real and imaginary impedance components and digitize results without any external hardware. Fabricated in a standard 0.5μm CMOS process, the IDC requires only 0.045mm² per readout channel. The power consumption is only 5.2μW per channel with a 3.3V supply and 200kHz reference clock. The compact size and low power of this circuit enable an IDC cell to be instantiated for every element in a sensor array to increase the interrogation throughput. Furthermore, the wide dynamic range (0.01-10kHz) and high accuracy of the IDC circuit permit it to support a diverse set of IS-based sensor interfaces.

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VII. REFERENCES