

# Online Calibration of Floating gate detectors for RFID Sensors

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**Abstract**—As the use of radio frequency identification (RFID) technology becomes widespread, one of the actively pursued research areas has been integration of smart sensors with RFID tags. These miniaturized devices when queried, transmit an identifier, subject to a specific condition of their environment. Applications of the sensors range from surveillance to biomedical systems. In this paper we will present a floating gate classifier that detects patterns of interest and enables or disables RF transmission on the tag. These classifiers consume minimal amount of energy and can be directly operated by scavenging power through inductive coupling. Applying online learning and calibration techniques to the classifier can compensate analog imperfections and mismatches in sensors. Results obtained from a prototype fabricated using standard 0.5 $\mu$ m CMOS process, are presented and the utility of learning on silicon is validated by demonstrated improvements in detection rates.

## I. INTRODUCTION

Radio-frequency identification (RFID) technology is posed to revolutionize different facets of technology ranging from inventory control to biosensor systems [1]. As a mature technology, RFID tags would provide near perfect supply chain visibility and in principle eliminate human errors in data collection. Integrating smart sensor technology with RFID tags will lead to "smart sensor tags" that will expand the utility of RFID technology to other fields of engineering and science, like surveillance and medicine. Of course this integration comes at a price of increased complexity and increased power consumption, a scarce resource for an RFID tag. Scavenging ambient energy resources like solar, thermal or vibrational energy can boost the power budget of smart sensor tags. This not only increases the longevity of the tags but also makes it autonomous and deployable for biosensor systems. The total power budget of the autonomous smart sensor tags range from  $0.9\mu\text{W}/\text{cm}^2$  to  $100\mu\text{W}/\text{cm}^2$  [3] illustrating the requirement of ultra low power circuits. To be a viable technology, these smart sensor tags, especially the sensory information processing circuits, have to be very low bandwidth devices in order to consume power as low as possible.

Low bandwidth circuits can be designed using low power analog circuits [2]. These low power circuits can eliminate high-end signal processing requirements. Low power analog circuits work with very small currents, so mismatch and noise can distort the original signal thus causing inaccuracies in measurement and classification. Sensor mismatch is another

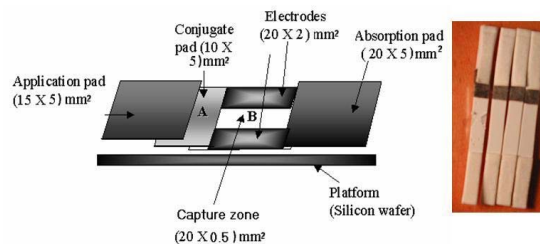


Fig. 1. Biosensor probe and its integration with silicon wafer

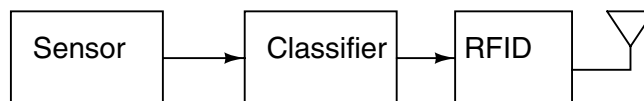


Fig. 2. Block diagram of the floating gate detector system. The classifier of detector consists of 8x8 floating gate matrix vector

source of error in measurement and classification systems. For example mismatch due to fabrication errors of biosensors are not very well streamlined or well controlled, so these biosensors show up to 10% variations in their characteristics [4], [5]. Typical biosensors are illustrated in fig. (1). A typical biosensor which has been used for this paper is shown in fig. (1) and described in [4], [5]. Impedance of these sensors changes in the presence of specific pathogens in its environment which can be transduced into current signals. A multi-channel biosensor therefore produces a vector of currents which can then be processed by a classifier as shown in fig. (2). The range of currents vary from femtoamperes to nanoamperes and can be sensed using translinear current mode circuits, which can be made extremely low power. This comes at an expense of increased mismatch and distortion, which has to be compensated [7].

Floating gates offer great flexibility in terms of programming of a current on to floating gate thus could be useful in compensation techniques [8]. Different computational blocks can be built using floating gate elements such as analog multipliers, memory storage, on-chip biases, and offset removals. Floating gates can be used to store currents that can be used as current references in data converters. Very recently floating gates are employed in imagers, filter banks and data

classifiers. Floating gate classifiers circuits have demonstrated good correction properties for any mismatches [9]. These require precise programming of floating gates to compensate for any mismatch. In this paper we show on-chip compensation technique that defines classifier characteristics without precise floating gate programming.

The paper is organized as follows. Section 2 describes the algorithm used for on-line calibration. Section 3 describes the architecture of the silicon prototype. Section 4 describes chip results followed by concluding remarks.

## II. ALGORITHM

Given a set of input training vector,  $x_i \in R^D$  where  $i = 1, 2, \dots, N$ ,  $D$  is the dimension of the values and  $N$  is the number of training points. Also are given  $y_i \in \{-1, +1\}$ , where  $i = 1, 2, \dots, N$ , which represents true class memberships. Aim is to find a hyperplane  $f(x) = \omega \cdot x + b$  which reduces total misclassification errors given by

$$\sum_{i=1}^N y_i \text{sign}(\omega \cdot x + b) \quad (1)$$

A simple adaptation rule to find such a hyperplane could be given by

$$\omega_i = \omega_{i-1} - \eta \Delta_i y_i \quad (2)$$

$$b_i = b_{i-1} - \eta y_i \quad (3)$$

where  $\eta$  is the learning rate and  $\Delta_i = \text{sign}(x_i)$

The update is made only when the classifier misclassifies a training point which is given by  $y_i(\omega \cdot x_i + b) < 0$ . The algorithm proceeds by repeatedly applying the rule and iterating through the training points till it converges or the number of errors reduces to minimum.

## III. ARCHITECTURE DESIGN

Fig. (2) shows basic block diagram of biosensor system.  $I_1, I_2, \dots, I_N$  are current outputs from sensors that would sense change in impedance of a biosensor. Since change in impedance is so small that it is difficult to track that change by measuring absolute value of current. Noise can severely affect the current measurements therefore differential currents are used to measure change in impedance. This change in current is still very small and is in the range of femtoampere to picoampere; so precise current mode measurement techniques are to be used to measure such small currents. If the transistors are operated in subthreshold region then we can get up to femtoamperes of current that can be programmed on to floating gates with precision. Thus measurement of currents using floating gates can prove to be very exciting.

A classifier matrix is formed by programming floating gate array with classifier weights. Depending on the type training samples, a classifier matrix can be programmed based on their impedance profiles thus offering great flexibility. RFID module transmits the classifier output to external receiver. Details of RFID module circuit are not discussed in this paper. Fig. (4) shows that output current  $I_{OUT}$  is given by

$$I_{OUT} = I_x * \exp[(kV_{gref} - kV_g)/U_T] \quad (4)$$

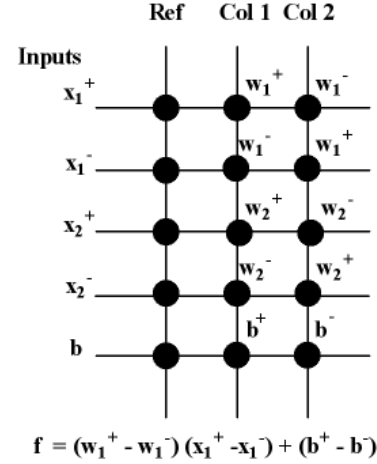


Fig. 3.  $f$  represents output current given by (6). Differential input currents are given to 5 rows of matrix given by  $x_1^+$ ,  $x_1^-$ ,  $x_2^+$ ,  $x_2^-$  and  $b$  in (6)

where  $I_x$  is input training current,  $V_{gref}$  and  $V_g$  are gate voltages of gates of reference cell and output cell respectively. After going through mathematical analysis it can be proved that output current  $I_{OUT}$  is given by ratio of currents flowing through output cell to reference cell times input current as given in (5).

$$I_{OUT} = I_x * (I_g / I_{gref}) \quad (5)$$

Thus we can obtain multiplication function if we operate transistors in subthreshold region. Programming floating gates with appropriate current values on them can vary the ratio ( $I_g / I_{gref}$ ). This ratio forms the weight of a classifier matrix. The current flowing through output node is a single quadrant multiplication current. To implement four-quadrant multiplication function, we use following differential decomposition as shown in fig. (3)

Let  $\omega$ ,  $x$  and  $b$  be represented by differential signals  $\omega^+, \omega^-, x^+, x^- \dots$  where  $\omega^+, \omega^-, x^+, x^- \dots > 0$ . Then the classifier function can be written as (6) where

$x^+$  and  $x^-$  are current inputs from biosensor,

$w^+$  and  $w^-$  are classifier weights and

$b^+$  and  $b^-$  are offset current constants and

$f$  is the output current.

$$f = f^+ - f^- = [w^+ - w^-][x^+ - x^-] + (b^+ - b^-) \quad (6)$$

As shown in fig. (3), one column computes  $f^+ = w^+ x^+ + b^+$  and the other column computes  $f^- = w^- x^- + b^-$ . Before any measurements are to be made, a classifier needs to be trained. It can be trained using known biosensor samples called training samples. Classifiers are affected by mismatches in transistors. So floating gates are helpful to train the classifier to avoid errors caused by mismatches. The other advantage of floating gate classifier is that it can be modified based on changes in environmental factors. This modification is done by changing the stored value of currents on these floating gates. With all floating gates programmed with calibrated classifier

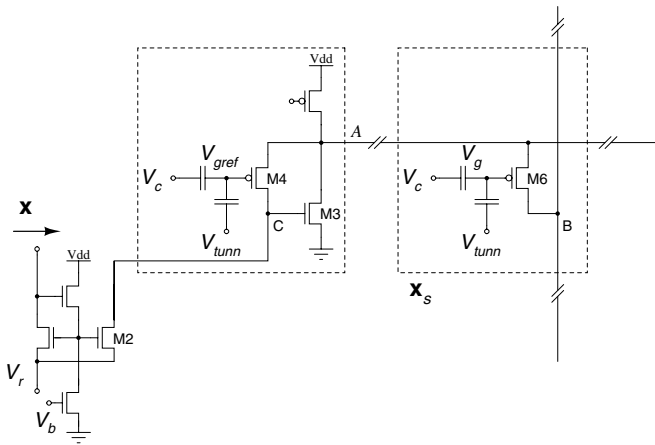


Fig. 4. Current input circuit stage

weights, a classifier hyperplane is formed that satisfies (1). This plane is a set of points that classifies the data into 2 sets. This classification can be made using any of the changing properties of biosensors. So if different properties of biosystems are to be tested then those cells will need different programming of weight values on floating gates of a matrix vector.

To create classifier hyperplane, all the cells are tunneled first to remove all the charge stored on floating gates. Then cells with weight  $w^+$  or  $w^-$  is injected with some current that will satisfy condition given by (2). Initially classifier is programmed with known current value that will try to satisfy classifier equation. Programming with some guessed current may not form an accurate hyperplane. With differential output of a classifier and known input signal, floating gate on one of the differential branch is injected with electrons till classifier satisfies condition given in (1). Injection is an iterative process so it may take lot of injection cycles before forming classifier hyperplane.

Fig. (4) shows current input circuit. The advantage of input circuit is that it can flow femtoampere of current through its reference current branch. Since  $V_b$  is biased such that gate voltage is tied to one threshold drop.  $V_r$  can be varied depending on input sensor potential range and thus help in getting femtoamperes of current as input. When two threshold voltage drop is seen between  $I_x$  ( Current sensor input X ) and  $V_r$  terminal, current starts flowing through the circuit. By having  $V_r$  as separate pin better control over the amount of current flowing through reference branch can be achieved.

#### IV. CHIP RESULTS

We fabricated our prototype chip in 0.5um CMOS technology available from MOSIS as shown in fig. (5). We built an array of  $8 * 8$  floating gate cells. At any given time 8 single ended or 4 differential biosensor currents can be applied as a input to floating gate array. The selection of each floating gate is done using row and column decoders that are made using serial shift register/decoder. All shift registers are pitch

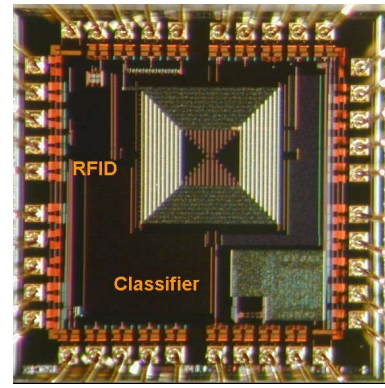


Fig. 5. Micrograph Structure:1.5mm \* 1.5mm

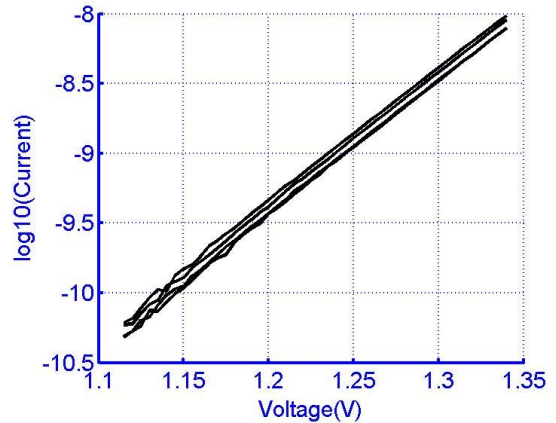


Fig. 6. Cells with same programmed value show different output current curves due to mismatch

matched with dimensions of floating gate cell so the design can be expanded by simple replication of basic building blocks.

Testing of a chip is done on custom-built PCB prototype board that provides interface with data acquisition card and Xilinx Spartan-3 FPGA board. All digital hardware interfaces are made through FPGA. Analog interface is provided by NIs data acquisition card. Matlab and Xilinx ISE are used for testing the chip.

Fig. (6) shows the output current seen by different cells in a row that are programmed with same currents. The output currents in the fig. (6) are given by (5) with all the weights assigned to 1. Ideally all cells should have same output current as input current. The differed values in output currents are because of mismatches in transistors. So when classifier is to be formed, every individual cell has to be fine programmed in order to form a classifier that would satisfy classifier equation with minimum errors.

Fig. (7) shows cells from same row that are programmed with different weights. Cell4: Cell3: Cell2: Cell1 are programmed with ratio 1:2:3:4. Thus, when transistors are operated in subthreshold region, multiplication function can be

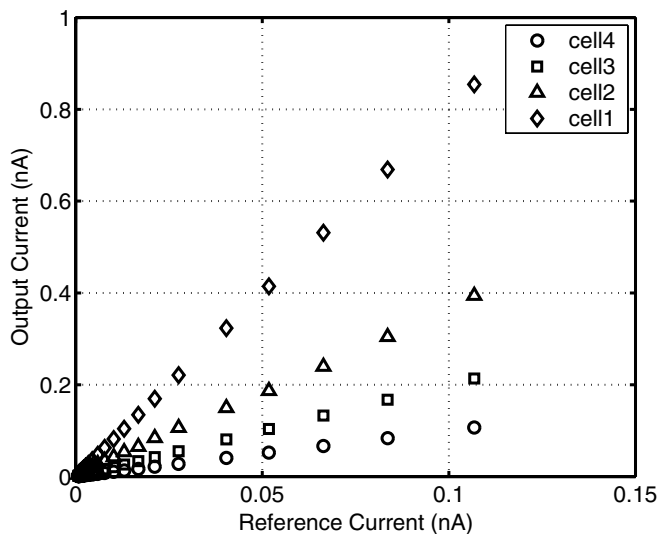


Fig. 7. Cells with weights multiples of cells 1 show that multiplication of current holds in subthreshold region

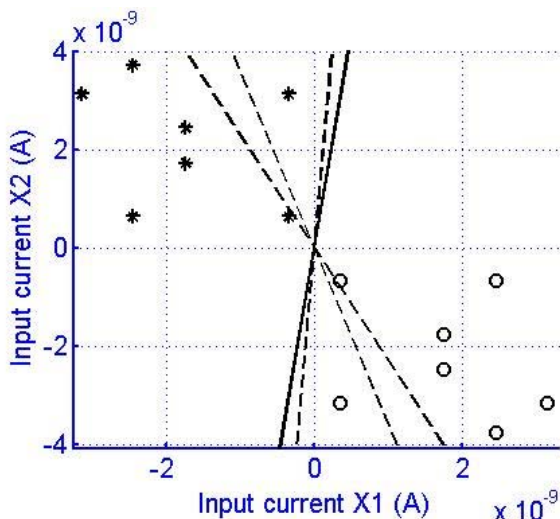


Fig. 8. Classifier hyperplane with errors are represented by dotted lines. After iterative injection of floating gates, classifier hyperplane rotates clockwise to satisfy conditions given by (1) and (2), the number of errors reduces minimizes which is represented by solid line

implemented.

Using all the result obtained above, a classifier can be programmed with known training samples. Fig. (8) shows the on-line adaptation procedure where the direction of the hyperplane is rotated when it encounters an error on one of the training points. With some stored values on floating gate, a hyperplane is formed that will try to classify given set of training samples. A hyperplane of a classifier that makes errors in classification is shown with dotted line. As floating gates are programmed with injection current, newly obtained hyperplane will try to rotate in clockwise direction in order to

reduce classification errors. After careful injection of currents in right cells, a classification hyperplane is formed that satisfies conditions given by (1), (2) and (3) given in algorithm. This hyperplane is represented by solid line that classifies all the data. Once the hyperplane is formed, any new set of input current can be classified under same environmental conditions.

## V. CONCLUSION

In this design hyperplane will rotate only in clockwise direction because currently electrons will be injected on to the gate. If selective tunneling can be used then rotation of hyperplane in both directions can be achieved. Floating gate cells can be very effectively used in vector matrix multiplications where inputs can be currents from array of biosensors. The presented chip is used for linear classifier but in future it can be used to make non-linear classifier used in support vector machines [10]. Structurally array of  $8 * 8$  floating gate cells took approximately  $175\mu\text{m} * 175\mu\text{m}$  area so idea of classifier can be extended up to  $64 * 64$  floating gate array with same die size of  $1.5\text{mm} * 1.5\text{mm}$  and thus can offer great deal on designing complex classifiers.

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