

Piezo-powered floating gate injector for self-powered fatigue monitoring in biomechanical implants.

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Abstract— In this paper we describe an implementation and modeling of a novel fatigue monitoring sensor based on integration of piezoelectric transduction with floating gate avalanche injection. The miniaturized sensor enables continuous battery-less monitoring and failure predictions of biomechanical implants. Measured results from a fabricated prototype in a 0.5 μ m CMOS process demonstrate excellent agreement with the theoretical model in computing cumulative statistics of electrical signals generated by the piezoelectric transducer. The power dissipation of the sensor is less than 1 μ W which makes it attractive for integration with biocompatible poly-vinylidene difluoride (PVDF) based transducers.

I. INTRODUCTION

Approximately 500,000 hip and knee replacements are performed each year in the United States. Although these implants exhibit excellent response during the initial rehabilitation period, fatigue and wear limits their success for long-term operation [1]. Monitoring of fatigue and wear has been previously shown to increase implant longevity by preventing mechanical failure through early intervention. Mechanical fatigue is the accumulation of damage in a structure under applied fluctuating stresses. Though the magnitudes of the applied stresses are less than the tensile strength of the material, the progressive fatigue damage may lead ultimately to mechanical failure. Fatigue life is defined as the number of load cycles necessary to induce failure and it depends on the level of fluctuating strain in the structure. Several fatigue prediction algorithms (eg Palmgren-Miner linear rule [5]) rely on counting the number and magnitude of loading cycles applied to a structure. The fatigue in the structure can then be estimated using the cumulative statistics of these applied loads.

Piezoelectric transducers not only provide a mechanism for sensing fatigue in a structure but also can be used for self-powering of the sensors [2]. Piezoelectric based self-powering for medical implants have several advantages over traditional battery powered techniques which suffer from limited life and complications due to biocompatibility. Poly-vinylidene difluoride (PVDF) is a piezoelectric plastic that is currently used for suture materials and has proven to be

biocompatible [3]. One of major disadvantage of PVDF is its very low mechano-electrical energy conversion. We have shown experimentally that the power generated from a PVDF sensor (shown in Figure 1) for a hip-implant monitoring is approximately 1 μ W [4]. Such low power levels pose several challenges for designing self-powered sensors, which include:

1. **Self-powered computation:** Energy to perform sensing and computation on the sensor has to be harvested from the converted mechanical signal.
2. **Non-volatile storage:** All the parameters of internal state variables (intermediate and final) have to be stored on a non-volatile memory to account for unavailability of power (i.e blackouts).
3. **Sub-microwatt operation:** All computation and storage functions have to be performed at sub-microwatt power dissipation levels to meet the power budget requirement of 1 μ W.

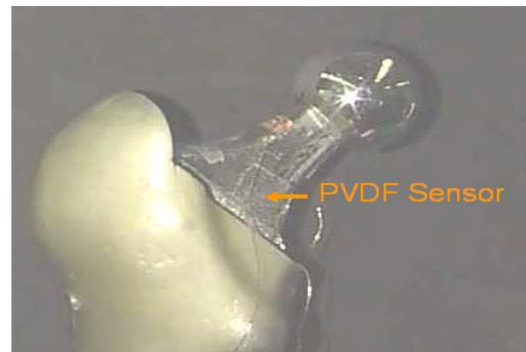


Figure 1: Stainless steel hip implant [4] showing PVDF sensor/generator attached for monitoring torsional loading.

In this paper we describe an implementation of a novel piezo-powered floating gate sensor that records cumulative statistics of stress undergone by a biomechanical implant. The concept behind the operation of the sensor is illustrated in Figure 2, where a piezo-electric transducer is coupled to a floating gate transistor. Based on the electrical signal generated by the transducer due to the induced stress, electrons are injected onto a floating node. The total charge accumulated on the floating gate could indicate the number of stress-strain events. This paper focuses on the design issues of a piezo-powered floating gate fatigue sensor. The important factors include: (a) the control of the rate of injection of the floating gate transistor, and (b) the

monotonic response of the sensor to the cumulative fatigue experienced by the implant. Further requirement is that the sensor operates for the life-time of the implant.

The paper is organized as follows: Section II models the response of a floating gate sensor and its electron injection characteristics. Section III describes a circuit implementation of the proposed sensor. Section IV describes preliminary results obtained from a fabricated prototype and section V concludes with some final remarks.

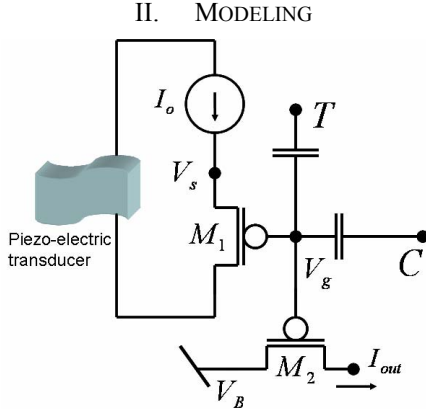


Figure 2: Simplified circuit model for piezo-driven floating gate sensor.

A simplified circuit model for the proposed piezo-driven floating gate sensor is shown in Figure 2. It consists of a floating gate (denoted by voltage V_g) which is coupled to the gates of an injection transistor M1 and a read-out transistor M2. The current delivered by the piezo transducer is limited by a current reference (I_0) which biases the transistor M1 in weak-inversion. The nodes C and T represent control and tunneling terminals [6]. In weak-inversion, the expression for source current through the pFET transistor M1 is given by:

$$I_0 = I_s e^{-\frac{V_g}{U_T}} e^{\frac{V_s}{U_T}} \quad (1)$$

where I_0 is the source current, I_s is a pre-exponential current, V_g is the floating gate voltage, κ is the coupling coefficient from floating gate to channel, U_t is the thermal voltage. For the fixed reference current I_0 , the gate current of M1 due to impact ionized hot-electron injection (IHEI) is given by:

$$I_g = \beta I_0 e^{V_s/V_{inj}} = -C \frac{\partial V_g}{\partial t} \quad (2)$$

Where β and V_{inj} are constants, and C is the total capacitance at the floating gate. Using equations (1) and (2), the following expression for V_g is obtained as a function of time:

$$V_g(t) = -\frac{1}{K_2} \log \left(K_1 K_2 \left(t + \frac{1}{K_1 K_2} e^{-K_2 V_{g0}} \right) \right) \quad (3)$$

where

$$K_1 = \left(\frac{\beta I_0}{C} \right) \left(\frac{I_0}{I_s} \right)^{\frac{U_t}{V_{inj}}} \quad (4)$$

$$K_2 = \frac{\kappa}{V_{inj}}$$

and V_{g0} is the initial gate voltage.

The floating gate voltage is mapped onto a read-out current I_{out} using the transistor M2. Because transistor M2 may not be in weak-inversion we use an EKV model [7] to compute the output current I_{out} as:

$$I_{out} = a^2 \log^2 \left(1 + \alpha e^{\frac{(-\kappa V_g + V_B)}{U_T}} \right) \quad (5)$$

where α and a are parameters of the model. The read-out current I_{out} is shown in figure 6 for parameters a and α , obtained experimentally. It can be seen from the model that the response of the circuit is monotonic and exhibits a saturating response. Therefore the model in Figure 2 could be used for calculating the total cumulative time a piezo-transducer was able to deliver a load current I_0 , which will be proportional to the cumulative stress period applied to the implant.

III. CIRCUIT IMPLEMENTATION

The piezo output is directly connected to a full wave rectifier, which has been implemented using a standard diode bridge. For the prototype n+ - p-substrate and p+ - n-well diodes were used, which naturally occur using electrostatic discharge (ESD) diodes. A storage capacitor was used at the output of the rectifier to filter out unwanted high-frequency components. The size of the capacitor provides a trade-off between total discharge time versus the voltage swing at the sensor. For the prototype an external capacitor (10nF) was chosen which led to voltage swing of up to 8V when 20V was generated by the piezoelectric transducer. A voltage over-protection and clamping circuitry was integrated at the output of the diode bridge to prevent damage due to unwanted piezoelectric surges.

The circuit used for implementing the floating gate reference array is shown in Figure 3. It consists of an array of floating gate transistors C2-C6, which act as non-volatile storage.

A floating gate is a poly-silicon gate surrounded by an insulator, which in standard semiconductor fabrication process is silicon-dioxide [6]. Because a floating gate is surrounded by high quality insulation any electrical charge injected onto this gate is retained for long intervals of time (> 8 years). When the floating gate is coupled to a gate of a transistor, as shown in Figure 4, the charge stored can be sensed as current flowing through the transistor. The charge on the gate can be modified using hot electron injection or through tunneling. Injection adds electrons to the floating gate as a result its potential decreases which leads to an

increase in the drain current through the transistor. For a pMOS transistor biased in weak-inversion drain-to-source voltages greater than 4.5V has been found to be sufficient for injection. Each floating gate transistor also has a tunneling capacitor which is used for removing electrons (erase operation) from the gate.

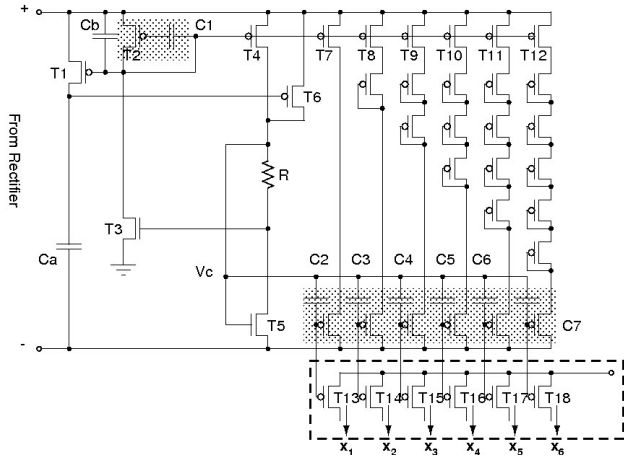


Figure3: Floating gate reference array

A reference current generator circuit is implemented using transistors T1-T5 and resistor R. In a standard current reference circuit the ratio of the pMOS current mirror transistors along with R determines the magnitude of the reference current. This implementation uses a floating gate transistor T2 and the reference current is determined by the charge injected onto the floating gate and the resistor value R. When all the transistors T2-T5 are biased in weak-inversion, the reference current through T4 is given by

$$I_{ref} \approx \frac{Q_f}{C_f R}$$

C1 and C_f is the total floating gate capacitance. By accurately controlling the amount of floating gate charge, Q_f , small increments of reference current can be generated.

Experiments with floating gate cells have indicated programming accuracy up to 100nA of current at a resolution of 0.1nA. Transistors T1, T6 form a start up circuit for the current reference. The reference current is used by mirrors T7-T12 to drive the source of floating gate transistors C2-C7. Voltage drop in each branch is controlled using diode connected pMOS transistors and ensures different drain-to-source voltage across each of floating gate cells C2-C7. During the pre-calibration stage each of the floating gate cells are programmed (using tunneling and injection) to store a fixed amount of charge and hence a fixed gate voltage across C2-C7. When a rectified voltage is presented across the supply terminals (+), the circuit generates a reference current and a stable voltage reference at node Vc. Depending on the magnitude of the rectified voltage different cells C2-C7 start injecting charge on its floating gate. The novelty of the circuit is in its ability to compensate for temperature variations, as evident from reference current expression which is independent of

temperature dependent parameters. Temperature compensation due to the current reference circuit has been validated through simulation and exhibits less than 2% variation over a 70°C variation in temperature. Even though this feature is not required during normal operation of the implantable device, it has been observed that for some implants (hip implants) repeated load cycles can dramatically increase the ambient temperature.

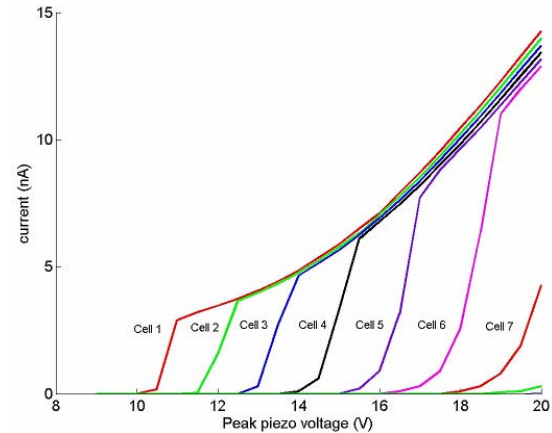


Figure4: Simulation results obtained using the floating gate reference array.

SpectreS based spice simulation of the current reference circuit demonstrates an activation profile of different floating gate cells C2-C7 at different peak amplitude. For this experiment a storage capacitor of 10nF was chosen, and the duration of the piezoelectric pulse excitation was set to 2 seconds. The circuit exhibits a start-up time of 100ms, which is sufficient for most structural engineering applications. The start-up however can be optimized by appropriately sizing the storage capacitor at the rectifier but at the expense of lower coupling voltage (rectifier). The simulation also shows poor current regulation of the reference circuit due to sub-threshold operation of the circuit but does not adversely affect the response of the sensor.

The results indicate that different floating gate cells in the array start injecting at different piezoelectric potential and therefore record cumulative amplitude statistics of the signal. The architecture therefore implements a self-powered flash data converter. The total charge accumulated on the floating gate is measured by sensing the current through the read-out transistors T13-T18.

IV. MEASURED RESULTS

A prototype floating-gate sensor was fabricated in a standard 0.5μm CMOS process. The micrograph of the prototype whose total area is 1.5mm x 1.5mm is shown in Figure 5.

The floating gate transistors were designed using a double polysilicon transistor with a minimum injection potential of 4.2V and an erase voltage of 15V. For preliminary experiments a signal generator was used to simulate the functionality of a piezoelectric transducer. Different voltage levels were applied at the floating gate array input, and the read-out current through transistor T13 was measured.

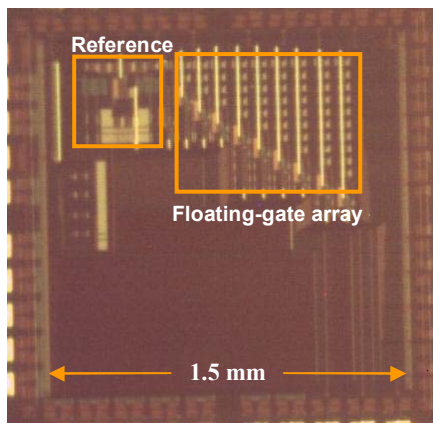


Figure 5: Micrograph of the prototype floating-gate sensor.

Figure 6 shows the current measured through transistor T13 for different voltages against the total duration of the applied input. The injection profiles for different voltages match with each other. This shows the importance of the current reference. Figure 6 also shows the output current obtained using the model developed in section II. There is a good match between the theoretical model and the measured results. The response is monotonic and approximately linear which demonstrates that the sensor can be used for computing total strain cycles experienced by a mechanical structure. The total power dissipated during the entire experiment was measured to be 320nW which is well below the power generated by a PVDF transducer ($1\mu\text{W}$). For long term monitoring it is critical that the measured current show a compressive non-saturating response (equivalent to logarithmic response). Long term monitoring experiments with the floating gate sensor have shown non-saturating response for up to 10^5 seconds demonstrating the effectiveness of current limiting transistors T7 in Figure 3.

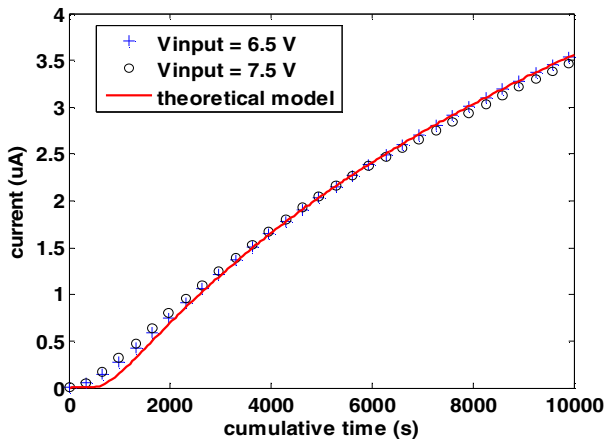


Figure 6: Measured response of a single floating gate reference element.

V. CONCLUSION

In this paper we have shown feasibility of a self-powered fatigue measuring system based on a combination of piezoelectric transduction and floating gate injection. We have presented preliminary results which indicate that the

response of the sensor is proportional to an equivalent total number of stress cycles experienced by a structure. The total power dissipation of the sensor is less than $1\mu\text{W}$ and we are currently integrating the device with PVDF based biomechanical implants.

REFERENCES

- [1] MA McGee et. Al. 'Implant retrieval studies of the wear and loosening of prosthetic joints: a review' *Wear*, Volume 241, Number 2, 31 July 2000, pp. 158-165(8)
- [2] GVB. Cochran, MW Johnson, MP Kadaba, F Vosburgh, MW Ferguson-Pell, VR Palmeiri 'Piezoelectric internal fixation devices: A new approach to electrical augmentation of osteogenesis' *Journal of Orthopaedic Research* Volume 3, Issue 4, Pages 508 – 513 (1985)
- [3] CC Enger, JH Kennedy, "An improved bioelectric generator," *Trans. Am. Soc. Artif. Intern. Organs*, vol. 10, pp. 373–377, Oct. 1964
- [4] Elvin N., Elvin A and Spector M., "Smart Orthopaedic Implant", US Patent No: 06034296.
- [5] S. Suresh, *Fatigue of Materials*, 2nd edition, Cambridge University Press, 1998.
- [6] C. Dorio, P. Hasler, B. Minch and C.A. Mead, "A Single-Transistor Silicon Synapse," *IEEE Trans. Electron Devices*, vol. 43 (11), Nov. 1996.
- [7] Enz, C.C, Krummenacher, F., and Vittoz, E.A, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, pp. 83-114, 1995.