

CMOS Analog Iterative Decoders Using Margin Propagation Circuits

Shantanu Chakrabarty
Department of Electrical and Computer Engineering
Michigan State University
East Lansing, MI 48824-1226
Email: shantanu@egr.msu.edu

Abstract—Analog iterative decoders offer several advantages over their digital counterparts in terms of speed and power consumption. The current state of art CMOS analog decoders uses MOS transistors biased in weak inversion which limits their speed of operation. In this paper a novel analog decoding network is presented which can operate with MOS transistor biased both in weak and strong inversion. The principle of operation is based on margin propagation algorithm which requires only addition, subtraction and thresholding operation which can be easily implemented in analog VLSI. A current mode implementation of the decoder is proposed which operates directly in log-likelihood space. This not only improves the speed of convergence for iterative decoding but also enhances the dynamic range of the decoder. Simulation based on a simple tail-biting trellis is presented that demonstrate the decoding characteristic and speed of operation of the proposed margin propagation network.

I. INTRODUCTION

Recently there has been a lot of interest in implementing iterative decoders (for eg. LDPC and turbo decoders) using analog VLSI [1], [2], [3]. Analog decoders are attractive compared to their digital counterparts because of their compactness and power efficiency [4]. Several analog VLSI implementations have been proposed in literature for implementing iterative decoders which either use high-end and expensive BiCMOS or SiGe process [3], or a relatively inexpensive CMOS process [1]. The underlying principle of operation of all analog decoders have been the use of trans-linear principles for implementing message passing [4], [6] algorithms like the popular sum-product algorithm [5] or the celebrated forward-backward algorithm [7]. Currently CMOS based implementations utilize MOS transistors biased in weak inversion, which limit their speed of operation. Moreover, most analog implementations require additional transformation circuits for mapping voltage encoded log-likelihood scores into current encoded probabilities. This transformation not only requires precise sample and hold techniques [1] for sub-threshold voltages but also introduces temperature dependencies.

In this paper a novel iterative decoding algorithm and its analog VLSI implementation is presented. The implementation is based on margin propagation principle [8] and offers following advantages:

- 1) The operation of the decoder does not rely on the bias condition of the MOS transistors. Therefore high-speed

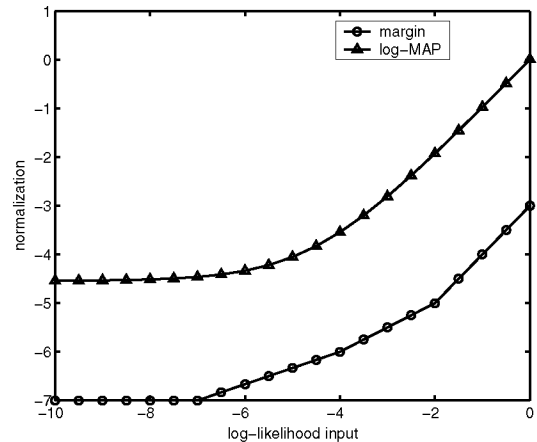


Fig. 1. Comparison of normalization factors computed using log-MAP normalization and reverse water-filling normalization.

operation can be achieved by biasing the transistors in strong inversion.

- 2) The decoding operation requires only addition, subtraction and thresholding which can be implemented using Kirchoff's current conservation principle and hence robust to temperature variations.
- 3) The decoding algorithm operates directly in log-likelihood space which leads to faster convergence and larger dynamic range. Use of current mode log-likelihood representation avoids precision requirements on sample and hold for analog decoding.
- 4) The proposed current mode design is compatible with existing current mode signaling techniques for on-chip and chip-to-chip communications.

A margin propagation network and its circuit implementation for maximum-a-posteriori (MAP) decoders has been proposed in [8]. However the algorithm in [8] can not be generalized to sum-product formulation [5] and the circuit implementation required low-current operation due to stability. In this work, the margin propagation principle has been extended to the framework based on sum-product decoding and its circuit implementation can be operated at much higher speed. The architecture of the network is modular, similar to sum-product based decoders and can be decomposed into basic

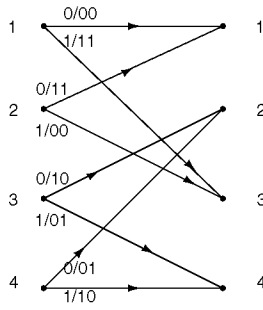


Fig. 2. A section of a trellis for a rate 1/2 code.

computational modules. The re-use of similar building blocks makes the design amenable to integration with digital design methods.

The paper is organized as follows: Section II describes the application of margin normalization to iterative decoders. The section also describes bit-error rate (BER) simulations obtained by implementing a turbo decoder using margin propagation. Section III describes a CMOS implementation of margin propagation for high-speed iterative decoders. Section IV describes simulation results obtained using the margin propagation circuits. Section V summarizes future directions with concluding remarks.

II. LOG-MAP AND MARGIN NORMALIZATION

The basic step in margin decoding algorithm is margin normalization. This section describes margin normalization and compares it with log-MAP normalization used in present iterative decoders. Given a set of log-likelihoods $\zeta_i, i = 1, \dots, N$, log-MAP normalization computes the normalization factor according to

$$Z = \log \sum_i e^{\zeta_i} \quad (1)$$

and the normalized score is $\bar{\zeta}_i = \zeta_i - Z$.

Margin normalization computes the normalization factor by solving the reverse water-filling equation [8] and is given by

$$\sum_i [\zeta_i - Z]_+ = \gamma \quad (2)$$

where $[\cdot]_+ = \max(\cdot, 0)$ denotes the thresholding operation and γ is a parameter of the reverse water-filling algorithm. The reverse water-filling procedure is described in [8] and is omitted for the sake of brevity. The equivalent normalized score is given by $\bar{\zeta}_i = [\zeta_i - Z]_+$. The comparison of both normalization factors are shown in Figure 1 which shows that margin normalization is a piece-wise linear approximation of log-MAP normalization, differing only by a constant.

III. LOG-MAP DECODING AND MARGIN PROPAGATION

Margin normalization principle can now be applied to iterative decoding of error correcting codes. Most error correcting codes can be represented using a trellis, which is a state transition graph exhibiting a Markovian property. A trellis of a

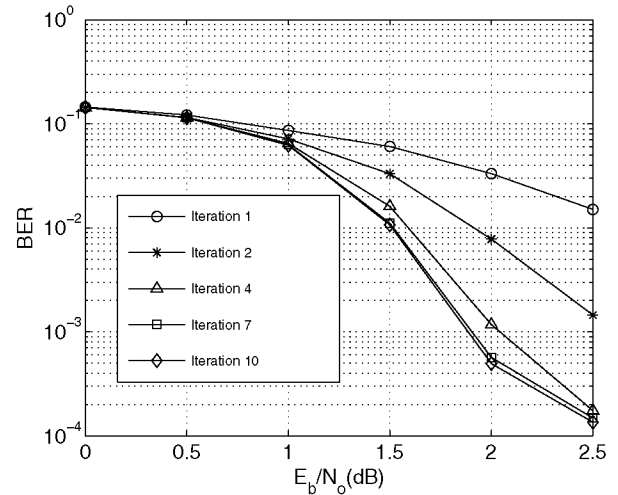


Fig. 3. BER curves for different iterations of turbo decoding algorithm using margin propagation.

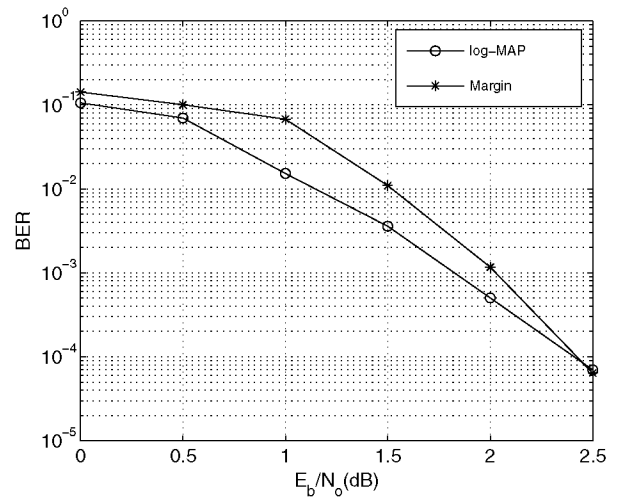


Fig. 4. Comparison of BER curves for a turbo decoder implemented using log-MAP decoding and margin propagation.

four state rate 1/2 encoder/decoder is shown in Figure 2. Each column of a trellis graph represents all possible system states (dots) $S_i, i = 1, \dots, N$ at a particular instant of time k and the branches represent state transitions between time instants $k-1$ and k . Each branch has an associated log-likelihood score $L_{ij}(k) = \log P(S_i, S_j; y_k)$ which is a function of received noisy observations y_k . Re-using the notation in [7], each state S_i is associated with a forward metric $\alpha_i(k)$ and a backward metric $\beta_i(k)$. In log-MAP decoding each metric is recursively computed according to

$$\alpha_i(k) = \nu_i(k) - \log \sum_p e^{\nu_p(k)} \quad (3)$$

$$\beta_i(k) = \nu'_i(k) - \log \sum_p e^{\nu'_p(k)} \quad (4)$$

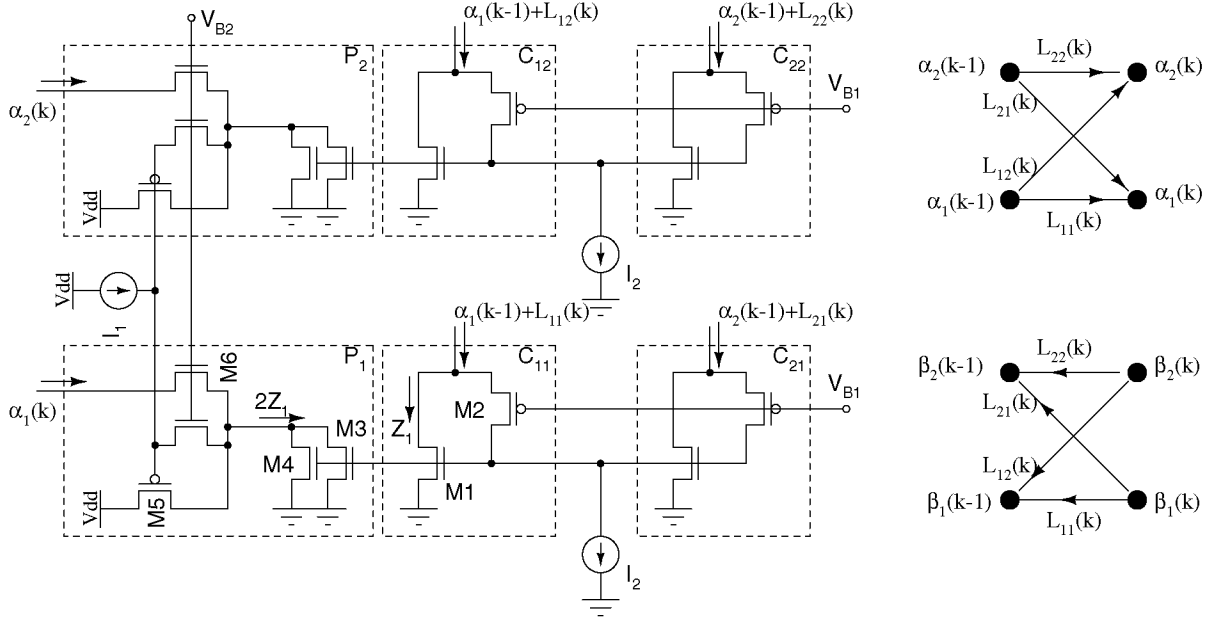


Fig. 5. CMOS implementation of a margin propagation network for a two-state fully connected trellis.

where $\nu_i(k) = \log \sum_j e^{\alpha_j(k-1) + L_{ij}(k)}$ and $\nu'_i(k) = \log \sum_j e^{\beta_j(k-1) + L_{ji}(k)}$.

Likewise forward and backward recursion for margin propagation can be derived by applying normalization equation (2) to equations (4) and (4) to obtain the following algorithm: Given two reverse water-filling parameters γ_1 and γ_2 , and an initial value of the forward-backward metrics $\alpha_i(0)$ and $\beta_i(0)$ for state $i = 1, \dots, S$

- 1) Compute the normalization factors ζ_i according to the reverse water-filling criterion $\sum_{j=1}^S [\alpha_j(k-1) + L_{ij}(k) - \zeta_i(k)]_+ = \gamma_1$.
- 2) Compute the normalization factor Z_k according to $\sum_{i=1}^S [\zeta_i(k) - Z_k]_+ = \gamma_2$.
- 3) Update $\alpha_i(k) \leftarrow [\zeta_i(k) - Z_k]_+$.
- 4) Compute the normalization factors ζ'_i according to the reverse water-filling criterion $\sum_j [\beta_j(k+1) + L_{ji}(k) - \zeta'_i(k)]_+ = \gamma_1$.
- 5) Update $\beta_i(k) \leftarrow [\zeta'_i(k) - Z_k]_+$.
- 6) Decoded state at time instant k is given by $S(\hat{k}) = \arg \max_i \alpha_i(k) + \beta_i(k)$.

Even though the above formulation has been described for a forward-backward algorithm, the technique is general and can be applied to any formulation based on sum-product techniques [5].

Margin propagation based iterative decoding was verified for turbo decoder, with a (7,5) recursive systematic coder (RSC) and with an inter-leaver size of 500 bits. Figure 3 shows the bit-error rate (BER) plot for different values of signal-to-noise (SNR) ratio. It shows that the turbo decoder implemented with margin propagation has convergence properties similar to log-MAP decoding, as the number of turbo iterations are increased. Figure 4 compares the BER for turbo-

decoder implemented with margin propagation and with log-MAP decoding after 10 turbo iterations. The result show that for reasonably high SNR values the performance of both schemes are similar.

IV. CIRCUIT IMPLEMENTATION

Margin normalization and propagation requires only addition, subtraction and thresholding operation. The reverse water-filling algorithm can therefore be implemented using a network of MOS transistors. A margin propagation network corresponding to forward-recursion procedure on a two state fully connected trellis is shown in Figure 5. The basic building block of the network consists of an inner-normalization block $C_{ij} : i, j = 1, \dots, S$ which implements row-wise reverse-water-filling algorithm according to step 1 of the margin propagation algorithm. The input to each row is a sum of currents representing the score $\alpha_j(k-1) + L_{ij}(k)$. Transistor M_2 is a feed-back transistor which sets the gate voltage of the normalization transistor M_1 . The current through M_1 then represents the normalization factor $\zeta_i(k)$ in step 1. Thresholding operation is achieved due to uni-directional flow of currents

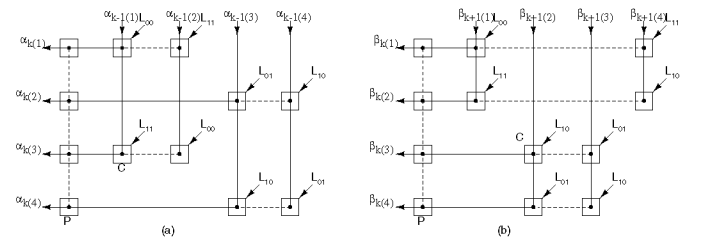


Fig. 6. Architecture of margin propagation decoder implementing the forward (a) and backward (b) recursion for the trellis in Figure 2.

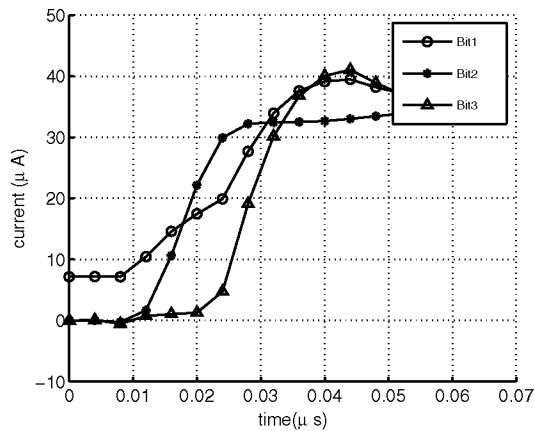


Fig. 7. Decoding characteristic of margin propagation based rate 1/2 decoder when the bits [1 1 1] are transmitted and received correctly.

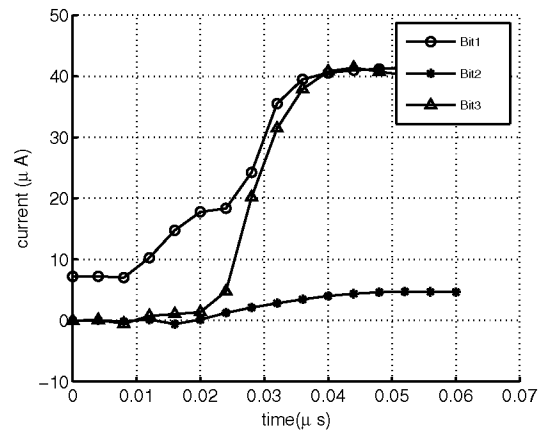


Fig. 8. Decoding characteristic when the bits are received incorrectly as [1 0 1].

through M_1 and M_2 . The network stabilizes when the water-filling criterion in step 1 of the algorithm is satisfied. The factors $\zeta_i(k)$ are re-normalized using another reverse water-filling circuit implemented by module $P_i : i = 1, \dots, S$. The implementation of P_i is similar to module C_{ij} except for the use of copy transistor M_6 . The current loading effect of M_6 is compensated by scaling the normalization factors $\zeta_i(k)$ by a factor of two using transistors M_4 and M_3 . The output of the modules P_i are normalized currents $\alpha_i(k)$ according to step 3 of the margin propagation algorithm. The backward recursion procedure can be implemented in a similar fashion using the trellis shown in Figure 5.

The modules C and P can now be re-used to construct any decoder that admits a trellis description. Figure 6 shows the architecture of a single section of a decoder implementing the forward and backward recursion using the trellis 2. The sections are cascaded to form a complete forward-backward decoding network. The module C processes the log-likelihood transition scores $L_{ab}(k) = \log P(a|y_1(k)) + \log P(b|y_2(k))$ based on received noisy bits $\{y_1(k), y_2(k)\}$. Decoded bits at time instant k are obtained from the trellis diagram 2 as

$$b(k) = \text{sign}(\Lambda_3(k) + \Lambda_4(k) - \Lambda_1(k) - \Lambda_2(k)) \quad (5)$$

$$\Lambda_i(k) = \alpha_i(k) + \beta_i(k) \quad (6)$$

V. RESULTS

A six stage trellis was constructed based on architecture 6 and its trellis description 2. All the log-likelihood scores L_{ab} were represented as currents and were presented to each stage of the trellis in parallel. The decoded bits $b(k), k = 1, \dots, 6$ were computed according to equation (6) using current summation and subtraction techniques. The current source corresponding to I_2 was biased to $10\mu A$ and the current I_1 was biased to $50\mu A$.

The rate 1/2 decoder was simulated in a $0.5\mu m$ CMOS process using spectreS. Figure 7 shows decoder output for three received bits received correctly. Figure 8 shows the decoder output when one of the bits was received incorrectly,

showing that the decoder can correct for the error in a single bit. The simulation results also indicate that the decoder can operate at speed greater than 100Mbps which is faster than sub-threshold based analog decoders [1].

VI. CONCLUSIONS

The paper introduced a novel iterative decoder based on margin propagation. The decoding principle is independent of the exponential characteristic of MOS transistors and therefore can be biased in strong inversion. A current mode circuit has been proposed and has been verified using a simple rate 1/2 code. Margin based decoders holds immense promise for future implementations as it only requires addition, subtraction and thresholding operation which can be easily implemented with nano-scale devices.

REFERENCES

- [1] Winstead, C., Jie Dai, Shuhuan Yu, Myers, C., Harrison, R.R., Schlegel, C. CMOS analog MAP decoder for (8,4) Hamming code, *Solid-State Circuits, IEEE Journal of* Volume 39, Issue 1, Jan. 2004 Page(s):122 - 131
- [2] M. H. Shakiba, D. A. Johns, and K. W. Martin, "BiCMOS circuits for analog Viterbi decoders," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, pp. 1527-1537, Dec. 1998.
- [3] Moerz, M., Gabara, T and Hagenauer, J, "An Analog 0.5μ Bi-CMOS tailbiting MAP decoder", *Solid-State Circuits Conference, 2000, ISSCC*, pp. 356-357, Feb 2000
- [4] Loeliger, H-A. et. al, "Probability Propagation and Decoding in Analog VLSI *International Symposium of Information Theory*, Cambridge, MA 1998.
- [5] F. R. Kschischang, B. J. Frey, and H.-A. Loeliger, "Factor graphs and the sum-product algorithm," *IEEE Trans. Inform. Theory*, vol. 47, pp. 498-519, Feb. 2001.
- [6] Lustenberger, F., Helfenstein, M. et. al, "An Analog VLSI Decoding Technique For Digital Codes", *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 424-427, vol.2 1999
- [7] L. R. Bahl, J. Cocke, F. Jelinek, and J. Raviv, "Optimal decoding of linear codes for minimizing symbol error rate," *IEEE Trans. Inform. Theory*, vol. 20, pp. 284-287, Mar. 1974.
- [8] S. Chakrabartty and G. Cauwenberghs, "Margin Propagation and Forward Decoding in Analog VLSI," *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS'2004)*, Vancouver Canada, May 23-26, 2004