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A sub-microwatt piezo-floating-gate sensor for long-term fatigue monitoring in biomechanical implants.

Nizar Lajnef[*], *Student Member IEEE*, Shantanu Chakrabartty[**] *Member IEEE*, Niell Elvin[*] *Member IEEE,* Alex Elvin[++] *Member IEEE*

Abstract— **In this paper we describe an implementation of a novel fatigue monitoring sensor based on integration of piezoelectric transduction with floating gate avalanche injection. The miniaturized sensor enables continuous battery-less monitoring and time-to-failure predictions of biomechanical implants. Measured results from a fabricated prototype in a 0.5µm CMOS process indicate that the device can compute cumulative statistics of electrical signals generated by piezoelectric transducer, while consuming less that 1µW of power. The ultra-low power operation makes the sensor attractive for integration with poly-vinylidene diflouride (PVDF) based transducers that have already proven to be biocompatible.**

I. INTRODUCTION

Fatigue and wear in biomedical implants remains a major clinical problem [1]. The monitoring of fatigue and wear has been previously shown to increase implant longevity, and can lead to early intervention to prevent mechanical failure. Piezoelectric transducers not only provide a mechanism for sensing fatigue in a structure but also can be used for self-powering of the sensors [2]. Piezoelectric based self-powering for medical implants have several advantages over traditional battery powered techniques which suffer from limited life and complications due to biocompatibility. Currently most research on implanted piezoelectric energy-harvesting has focused on the use of lead zirconate titanate (PZT) piezoelectrics because of their high mechano-electrical energy conversion efficiency [2]. However the biocompatibility of PZT remains unknown. On the other hand poly-vinylidene diflouride (PVDF) is a piezoelectric plastic that is currently used for suture materials and has proven to be biocompatible [3]. One of major disadvantage of PVDF is its very low mechano-electrical energy conversion. We have shown experimentally that the power generated from a PVDF sensor (shown in Figure 1) for a hip-implant monitoring is approximately 1µW [4]. Such low power levels pose several challenges for designing self-powered sensors, which include:

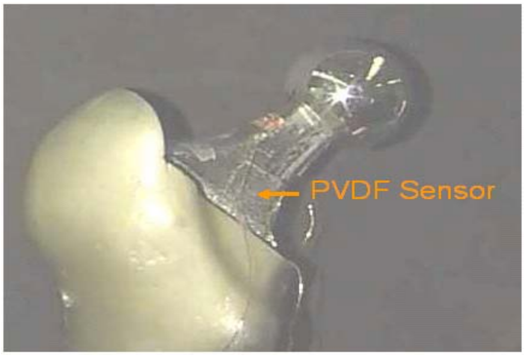

Figure 1: Stainless steel hip implant [4] showing PVDF sensor/generator attached for monitoring torsional loading.

1. **Self-powered computation**: Energy to perform sensing and computation on the sensor has to be harvested from the converted mechanical signal.
2. **Non-volatile storage**: All the parameters of internal state variables (intermediate and final) have to be stored on a non-volatile memory to account for unavailability of power.
3. **Sub-microwatt operation**: All computation and storage functions have to be performed at sub-microwatt power dissipation levels to meet the power budget requirement of 1µW.

In this paper we describe an implementation of a novel self-powered piezo-floating gate sensor that records cumulative statistics of stress undergone by a biomechanical implant. The statistics can then be used for time-to-failure prediction based on existing counting algorithms. The paper is organized as follows: Section II provides a background on fatigue and time-to-failure prediction algorithms. Section III describes a circuit implementation of the sensor. Section IV describes preliminary results obtained from a fabricated prototype and section V concludes with some final remarks.

II. BACKGROUND

A. *Fatigue monitoring algorithms*

Mechanical fatigue is the accumulation of damage in a structure under applied fluctuating stresses. Though the magnitudes of the applied stresses are less than the tensile strength of the material, the progressive fatigue damage may lead ultimately to mechanical failure.

Fatigue life is defined as the number of constant amplitude load cycles necessary to induce failure in an initially undamaged component. Generally, the fatigue life of a

The authors are with Civil and Environmental Engineering[*] and Electrical and Computer Engineering Department[**], Michigan State University, East Lansing, MI 48824 USA (Phone: 517-432-5679; fax: 517-353-1980; e-mail: lajnefni@msu.edu) and with Department of Civil and Environmental Engineering, University of Witwatersrand[++], Johannesburg, South Africa.

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mechanical component under cycling applied load depends on the level of fluctuating strain in the structure. This can be represented by the S-N curve (Figure3), which is obtained using experimental measurements. In the S-N curve, S is the mechanical strain level (Δε) in the component under a harmonic load, and N is the number of cycles that causes failure of the component at that strain level.

The S-N curves can be used directly to estimate the fatigue life under constant amplitude harmonic load conditions. However, in most real applications the applied load is not cyclic. The simplest approach to model fatigue behavior under variable amplitude load condition involves the concept of cumulative damage, which can be described using the Palmgren-Miner linear rule (Equation 1) [5]

$$\sum_{i=1}^{m}\frac{n_i}{N_{fi}}=1 \qquad (1)$$

where n_i denotes total number of events when the electric signal generated by the piezoelectric transducer exceeded a threshold a_i. Miner's rule assumes that each strain cycle of a given magnitude consumes $1/N_{fi}$ of the total fatigue life, where N_{fi} is the fatigue life of the specimen at the given strain amplitude (obtained from the S-N curve). A major step in the implementation of this approach is the identification of different loading events that contribute to fatigue damage. Counting algorithms are used to reduce any loading spectra to a series of equivalent stress-strain states. The experimental data for each stress-strain state is implemented with the Palmgren-Miner's rule to provide a summation of fatigue damage. Several empirical cycle counting methods have been developed for different applications. For the purpose of this study, a modified level-crossing peak counting method is used. This method consists on detecting, and summing the maximum level reached by different peaks of the applied strain function. Other counting algorithms are described in [5].

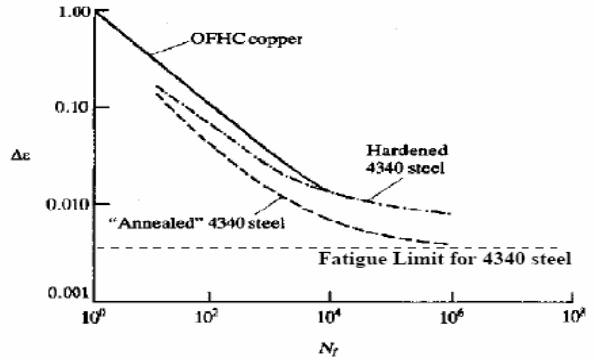

Figure3: example of S-N curves

III. SYSTEM ARCHITECTURE

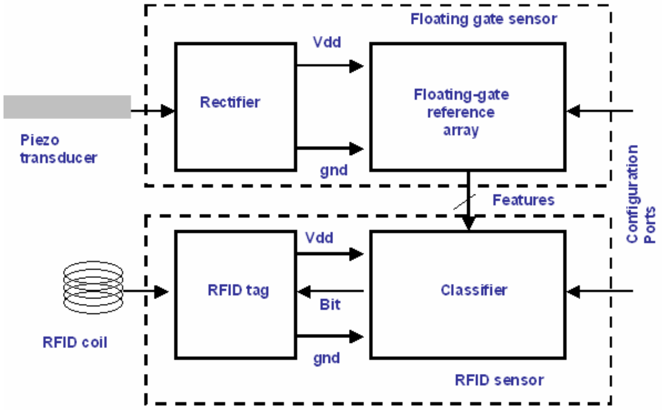

Figure4: Integration of the proposed floating gate sensor with an RFID interface.

The system level architecture of the proposed sensor is shown in Figure 4. It consists of a self-powered sub-system called a floating gate sensor that continuously records the statistics of a piezoelectric signal. The sub-system consists of a full-wave rectifier that generates un-regulated supply voltages (vdd and gnd). The supply voltages are used by a floating gate reference array to compute the amplitude and duration statistics of the rectified signal. The array then updates the internal variables which represent cumulative history of the mechanical strain cycles experienced by the structure. The floating gate sensor is self-powered and extracts all its operational energy from the rectified signal. The cumulative statistics is stored as charge on non-volatile memory and is used as features for an RFID sensor sub-system. We have previously described the RFID sub-system that consisted of a classifier processing cumulative features to produce a single confidence metric [6]. For this sensor the confidence metric indicates degree of fatigue in the structure. The powering and operation of the RFID-subsystem is completely asynchronous and derives its power through RF coupling from an external interrogator.

IV. CIRCUIT IMPLEMENTATION

A. Piezo-floating gate sensor

The full wave rectifier has been implemented using a standard diode bridge. For the prototype n+ - p-substrate and p+ - n-well diodes were used, which naturally occur using electrostatic discharge (ESD) diodes. A storage capacitor was used at the output of the rectifier to filter out unwanted high-frequency components. The size of the capacitor provides a trade-off between total discharge time versus the voltage swing at the sensor. For the prototype an external capacitor (10nF) was chosen which led to voltage swing of up to 8V for 20V generated by the piezoelectric transducer. A voltage over-protection and clamping circuitry was integrated at the output of the diode bridge to prevent damage due to unwanted piezoelectric surges.

The circuit used for implementing the floating gate reference array is shown in Figure 5. It consists of an array of floating gate transistors C2-C6, which act as a non-volatile storage.

A floating gate is a poly-silicon gate surrounded by an insulator, which in standard semiconductor fabrication process is silicon-dioxide [7]. Because a floating gate is surrounded by high quality insulation any electrical charge injected onto this gate is retained for long intervals of time (> 8 years). When the floating gate is coupled to a gate of a transistor, as shown in Figure 5, the charge stored can be sensed as current flowing through the transistor. The charge on the gate can be modified using hot electron injection or through tunneling. Injection adds electrons to the floating gate as a result its potential decreases which leads to an increase in the drain current through the transistor. For a pMOS transistor biased in weak-inversion drain-to-source voltages greater than 4.5V has been found to be sufficient for injection. Each floating gate transistor also has a tunneling capacitor which is used for removing electrons (erase operation) from the gate.

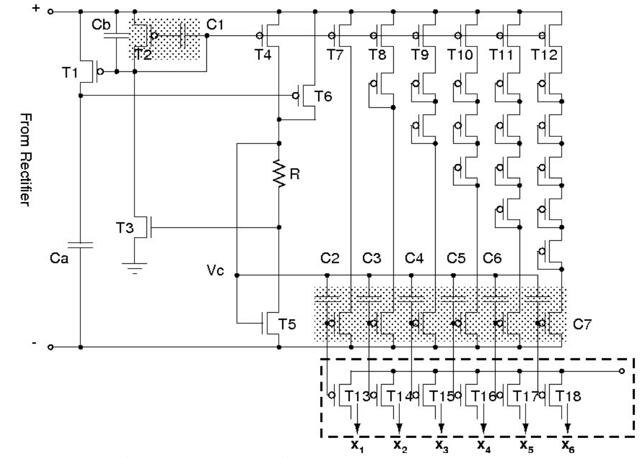

Figure5: Floating gate reference array

A reference current generator circuit is implemented using transistors T1-T5 and resistor R. In a standard current reference circuit the ratio of the pMOS current mirror transistors along with R determines the magnitude of the reference current. This implementation uses a floating gate transistor T2 and the reference current is determined by the charge injected onto the floating gate and the resistor value R. When all the transistors T2-T5 are biased in weak-inversion, the reference current is through T4 is given by $I_{ref} \approx \frac{Q_f}{C_f R}$ where Q_f is the charge stored on the floating gate C1 and C_f is the total floating gate capacitance. By accurately controlling the amount of floating gate charge, Q_f, small increments of reference current can be generated.

Experiments with floating gate cells have indicated programming accuracy up to 100nA of current at a resolution of 0.1nA. Transistors T1, T6 form a start up circuit for the current reference. The reference current will be used by mirrors T7-T12 to drive the source of floating gate transistors C2-C7. Voltage drop in each branch will be controlled using diode connected pMOS transistors and will ensure different drain-to-source voltage across each of floating gate cells C2-C7. During the pre-calibration stage each of the floating gate cells are programmed (using tunneling and injection) to store a fixed amount of charge, hence a fixed gate voltage across C2-C7. When a rectified voltage is presented across the supply terminals (+-), the circuit generates a reference current and a stable voltage reference at node Vc. Depending on the magnitude of the rectified voltage different cells C2-C7 start injecting charge on its floating gate. The novelty of the circuit is in its ability to compensate for temperature variations, as evident from reference current expression which is independent of temperature dependent parameters. Temperature compensation due to the current reference circuit has been validated through simulation and exhibits less than 2% variation over a 70°C variation in temperature. Even though this feature is not required during normal operation of the implantable device, it has been observed that for some implants (hip implants) repeated wear and tear can dramatically increase in ambient temperature.

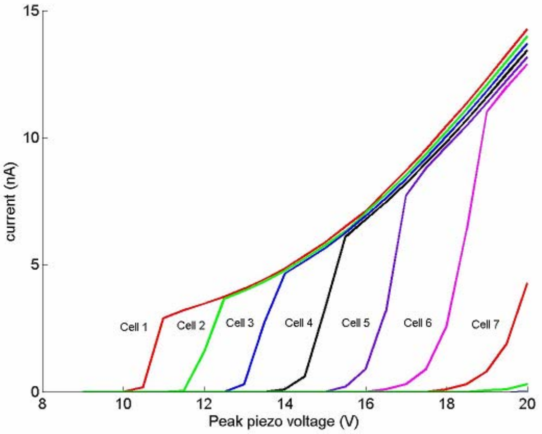

Figure6: Simulation results obtained using the floating gate reference array.

SpectreS based spice simulation of the current reference circuit demonstrates an activation profile of different floating gate cells C2-C7 at different peak amplitude. For this experiment a storage capacitor of 10nF was chosen, and the duration of the piezoelectric pulse excitation was set to 2 seconds. The circuit exhibits a start-up time of 100ms, which is sufficient for most structural engineering applications. The start-up however can be optimized by appropriately sizing the storage capacitor at the rectifier but at the expense of lower coupling voltage (rectifier). The simulation also shows poor current regulation of the reference circuit due to sub-threshold operation of the circuit but does not adversely affect the response of the sensor.

The results indicate that different floating gate cells in the array start injecting at different piezoelectric potential and therefore record cumulative amplitude statistics of signal. The architecture therefore implements a self-powered flash data converter. The total charge accumulated on the floating gate is measured by sensing the current through the read-out transistors T13-T18.

V. MEASURED RESULTS

A prototype floating-gate sensor was fabricated in a standard 0.5µm CMOS process. The micrograph of the prototype whose total area is 1.5mm x 1.5mm is shown in Figure 8.

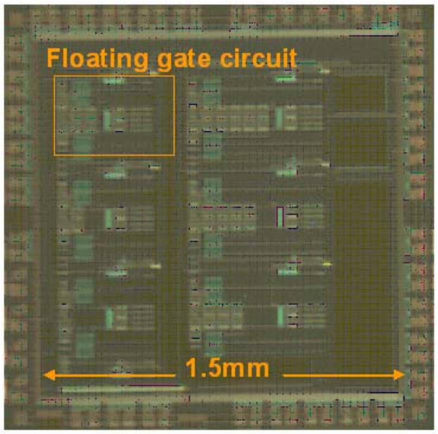

Figure7: Micrograph of the prototype floating-gate sensor.

The floating gate transistors were designed using a double polysilicon transistor with a minimum injection potential of 4.2V and an erase voltage of 15V. For preliminary experiments a signal generator was used to simulate the functionality of a piezoelectric transducer. Different voltage levels were applied at the floating gate array input, and the read-out current through transistor T13 was measured.

Figure 8 shows the current measured through transistor T13 for different voltages against the total duration of the applied input. The injection profiles for different voltages are relatively close to each other due to current reference based injection architecture. The response is monotonic and approximately linear which demonstrates that the sensor can be used for computing total strain cycles experienced by a mechanical structure. The total power dissipated during the entire experiment was measured to be 320nW which is well below the power generated by a PVDF transducer (1µW). For long term monitoring it is critical that the measured current show a compressive non-saturating response (equivalent to logarithmic response). Long term monitoring experiments with the floating gate sensor have shown non-saturating response for up to 10^5 seconds demonstrating the effectiveness of current limiting transistors T7 in Figure 5.

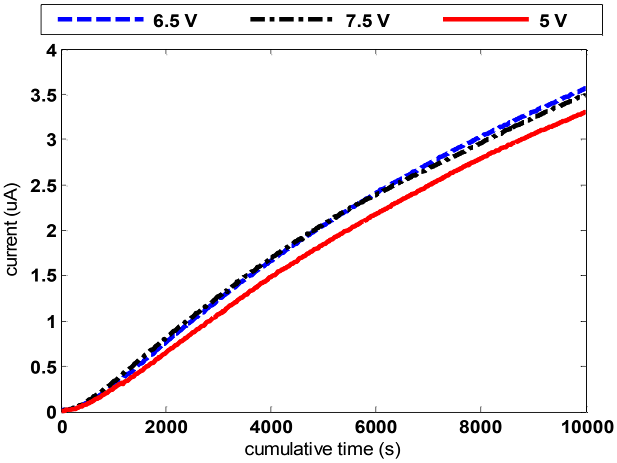

Figure 8: Measured response of a single floating gate reference element.

VI. CONCLUSION

In this paper we have shown feasibility of a self-powered fatigue measuring system based on a combination of piezoelectric transduction and floating gate injection. We have presented preliminary results which indicate that the response of the sensor is proportional to an equivalent total number of stress cycles experienced by a structure. The total power dissipation of the sensor is less than 1µW and we are currently integrating the device with PVDF based biomechanical implants.

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