

# Low-threshold Voltage Multipliers based on Floating-gate Charge-pumps

Chenling Huang

Department of Electrical and Computer Engineering  
Michigan State University  
East Lansing, U.S.A.  
huangc33@egr.msu.edu

Shantanu Chakrabarty

Department of Electrical and Computer Engineering  
Michigan State University  
East Lansing, U.S.A.  
shantanu@egr.msu.edu

**Abstract**—The paper presents a low-threshold voltage multiplier circuit that can be used for harvesting energy from ambient radio-frequency (RF) signals. At the core of the circuit is a charge-pump based on CMOS floating-gate transistor diodes (FGTD) whose threshold voltage can be adjusted using indirect programming. We show that the diodes can achieve threshold voltages less than 50mV, which is typically less than the conventional Schottky diodes fabricated in an equivalent process. A prototype of a 5-stage charge-pump is fabricated in a standard 0.5- $\mu\text{m}$  CMOS process ( $V_{th} = 0.7\text{V}$  and  $-0.9\text{V}$  for nMOS and pMOS transistors respectively). Measurement results validate the functionality of the prototype for multiplying and regulating sub-threshold input signals. Using a 5-stage charge-pump we demonstrate operation at less than 300mV input signal range with an operating frequency ranging from 1-4MHz.

## I. INTRODUCTION

Powering of in-vivo monitoring devices using ambient radio-frequency energy offers numerous advantages for long-term monitoring over implanted batteries which have limited life-span. However, RF signal propagating through living tissue suffers significant degree of attenuation and hence in-vivo RF powering using an ex-vivo portable transponder poses a significant challenge. For example, it has been shown that the attenuation caused by the skin alone could be more than 50dB (for a 4MHz RF signal) [1][2]. Given the limitations imposed on the impedance of the RF antenna, its distance from the RF source and FCC regulations on radiation leakage, the voltage induced across the input terminal of the implanted coil is typically less than 300mV. Most RF power harvesting systems use a form of voltage multiplying charge-pumps for generating and regulating higher voltage levels which is required for operating auxiliary CMOS circuitry on the monitoring device [3]-[7].

The fundamental principle behind the operation of a voltage multiplier circuit is to exploit the non-symmetrical impedances seen across two terminals of a circuit element. Figure 1 shows one of popular topology of a five stage voltage multiplier that uses the non-symmetric properties of a diode

which (under ideal conditions) allows unidirectional flow of current. In the positive phase of the input signal, the input current flows through diode  $D1$  to charge capacitor  $C1$ . The final voltage across  $C1$  will be  $V_{amp} - V_{th}$ , where  $V_{amp}$  is the amplitude of the input RF signal and  $V_{th}$  is the threshold of the diode. In the negative phase of the input, diode  $D1$  blocks the flow of current and capacitor  $C2$  will be charged through capacitor  $C1$  and Diode  $D2$  which results in a potential difference across the capacitor  $C2$  equals  $2\alpha(V_{amp} - V_{th})$ . The parameter  $\alpha < 1$  models the imperfect charge transfer from  $C1$  to  $C2$  (due to charge sharing). Accordingly, the voltage output of an  $N$ -stage multiplier can be expressed as

$$V_{out} = N\alpha(V_{amp} - V_{th}). \quad (1)$$

Thus, from equation (1) it can be seen that one of the important parameters that determines the operational limit of the voltage multiplier is the threshold voltage  $V_{th}$ . For a standard MOSFET diode and a p-n junction fabricated in a standard CMOS process,  $V_{th}$  is typically 700mV and hence obviates its use in low-threshold voltage multipliers. As a result, different diode topologies have been proposed in literature to reduce the threshold of the multiplier circuit.

The first approach is to use the special process with low-threshold or even zero-threshold transistor [3], but that will increase the cost of the fabrication. The second approach is to use Schottky diodes which typically have a lower threshold

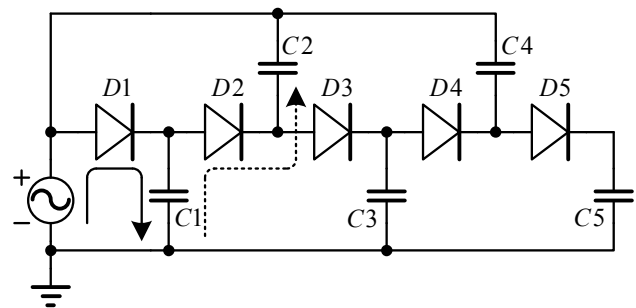


Figure 1. Structure of a basic 5-stage voltage multiplier charge-pump.

( $V_{th} = 100\text{mV}$ ) [4]. However, Schottky diodes ( $V_{th} = 100\text{mV}$ ) suffer from large mismatch errors and may not be compatible with many standard CMOS processes. Another approach for reducing the threshold is to use active circuitry for compensating the threshold [5] of a MOSFET transistor. However, biasing and power dissipation considerations limit the application of this approach for designing voltage multipliers in power harvesting systems.

In this paper, we propose a low-threshold voltage multiplier based on floating-gate transistors. The floating-gate transistors have been extensively used in the Electrically Erasable Programmable Read-Only Memory (EEPROM) where hot carrier injection and Fowler-Nordheim (FN) tunneling have been used to change the threshold voltage of the transistor and use the principle for data storage. In this work, the floating-gate transistors are programmed to operate at low-threshold voltage ( $< 300\text{mV}$ ) which is then used to amplify the diode charging current without significantly affecting the reverse leakage current. The paper also presents a calibration method that is used for initializing the voltage multiplier to operate at arbitrary input voltage levels. The paper is organized as follows. Section II proposes the circuit model for a floating-gate transistor diode (FGTD) and describes the programming procedure for a single FGTD. Section III presents the implementation and the measurement results for the prototype. Section VI concludes the paper with some final remarks.

## II. FLOATING-GATE TRANSISTOR DIODE

### A. Circuit Model

The fundamental building block of the proposed charge-pump is a floating-gate transistor diode (FGTD) which is shown in Fig. 2. It consists of a pMOS floating-gate transistor with its floating-gate ( $g$ ) being capacitively connected to node  $s$ . The schematic in Fig. 2 also shows two parasitic diodes,  $D1$  is formed between the drain and bulk of the pMOS transistor and  $D2$  is formed between the bulk and the substrate (which is always connected to ground). Then the total current flowing through the FGTD can be expressed as,

$$I_{total} = I_{ds} + I_{D1} + I_{D2} \quad (2)$$

where  $I_{ds}$  is the current flowing from node  $d$  to node  $s$  for the pMOS transistor,  $I_{D1}$  and  $I_{D2}$  are the leakage currents of the two diodes. For the voltage levels of interest, the FGTD is will operate in the weak-inversion region where the drain-to-source current can be expressed as [8],

$$I_{ds} = I_0 \frac{W}{L} \exp\left(-\frac{V_{gb}}{n \cdot U_T}\right) \left[ \exp\left(\frac{V_{db}}{U_T}\right) - \exp\left(\frac{V_{sb}}{U_T}\right) \right] \quad (3)$$

where  $I_0$  is the pre-exponential current of the pMOS transistor,  $W/L$  is the aspect ratio,  $n$  is the slope factor. All the voltages are referred to the bulk which is denoted by the subscript  $b$ . The voltage of the bulk is shown in Fig. 2 as the same as the source voltage. Since the bulk voltage is considered higher than the ground, diode  $D2$  is reversed biased the current  $I_{D2}$  can be ignored compared to the total current. The current flow through diode  $D1$  can be expressed as,

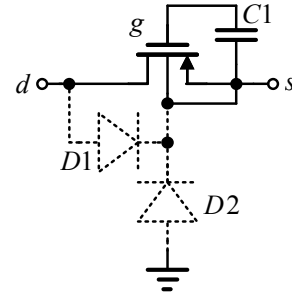


Figure 2. Schematic of FGTD with parasitic diodes.

$$I_{D1} = I_S \left[ \exp\left(\frac{V_{db}}{U_T}\right) - 1 \right] \quad (4)$$

where  $I_S$  is the pre-exponential current of the diode and  $U_T$  is the thermal voltage (26mV). Apply (3) and (4) into (2), and noting that the bulk is connected to the node  $s$ , the total current of the FGTD can be written as,

$$\begin{aligned} I_{total} &= I_0 \frac{W}{L} \exp\left(\frac{\Delta V}{n \cdot U_T}\right) \left[ \exp\left(\frac{V_{ds}}{U_T}\right) - 1 \right] + I_S \left[ \exp\left(\frac{V_{ds}}{U_T}\right) - 1 \right] \\ &= \left[ I_0 \frac{W}{L} \exp\left(\frac{\Delta V}{n \cdot U_T}\right) + I_S \right] \times \left[ \exp\left(\frac{V_{ds}}{U_T}\right) - 1 \right] \end{aligned} \quad (5)$$

where  $\Delta V$  represents the voltage drop between the source and gate depending on the charge stored on  $C1$ . Equation (5) represents an I-V characteristic of a diode, with an amplification factor that is proportional to the voltage  $\Delta V$  which can be used to adjust the threshold voltage of the FGTD.

### B. Programming Procedure

There are two different approaches to modify the voltage  $\Delta V$  on the floating-gate node. Impact-ionized hot-electron injection (IHEI) is a mechanism to add electrons which occurs when a high electrical field is applied across the drain-to-channel region [9]. A complementary method to remove electrons from the floating-gate node is FN tunneling which is based on a quantum mechanical transport phenomenon [10]. To ensure that the voltage  $\Delta V$  can be programmed without using any additional switches to isolate each of the FGTD in the charge-pump we use an indirect programming method as described in [11].

The setup is shown in Fig. 3, where an auxiliary transistor  $M_p$  shares the common floating-gate node with  $M1$ . The terminal  $V_{cg}$  is used to set a constant DC level for the floating-gate node through capacitor  $C3$ . For this prototype,  $V_{cg}$  nodes are all connected to the ground. In the  $0.5\text{-}\mu\text{m}$  CMOS process, the voltage difference between terminals  $V_d$  and  $V_s$  is measured to be at least 4.2V to trigger the onset of IHEI. The tunneling terminal  $V_{tun}$  is coupled to the floating-gate node through capacitor  $C2$  which is formed by the overlap between the active area and gate region. A large DC voltage (typically 15V for a  $0.5\text{-}\mu\text{m}$  CMOS process) is necessary to apply to  $V_{tun}$  for removing electrons. All the change of the floating-gate node can be measured at terminal  $V_{fg}$  through a unit buffer.

Both the simulation and measurement results are shown in Fig. 4 for the threshold programming of the FGTD, which are shown to be in good agreement. The I-V curves of the diode are shown for different values of  $\Delta V$  between the source and gate as measured using a read-out buffer (see Fig. 3). It can be seen from Fig. 4 that the threshold voltage of the FGTD can be made as low as 50mV. Also, from the measurement results it can be seen that the indirect programming provides a good control over adjusting the threshold of the FGTD device.

### III. IMPLEMENTATION AND MEASUREMENT

A 5-stage voltage multiplier charge-pump circuit based on Fig. 1 was prototyped on a standard 0.5- $\mu\text{m}$  CMOS process. Fig. 5 shows a micrograph of the charge-pump which occupies an area of  $100\mu\text{m} \times 700\mu\text{m}$ . The aspect ratios of the floating-gate transistor were chosen to be  $3\mu\text{m}/600\text{nm}$  and the load capacitors of the charge-pump (C1-C5 in Fig. 1) were designed to be 1pF.

#### A. Initialization Procedure

Before the charge-pump can be used for voltage multiplication, the threshold voltages of all the FGTDs have to be equalized to obtain the optimal DC output voltage. We use the following calibration algorithm to program the voltages  $\Delta V$  on each of the FGTD:

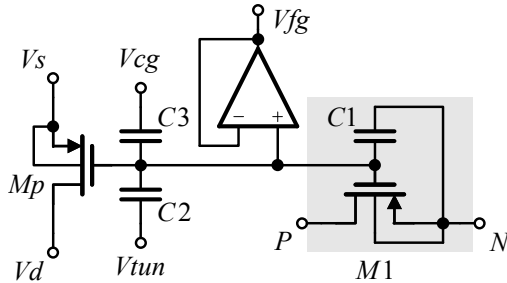


Figure 3. The FGTD with an auxiliary programming transistor for adjusting its threshold.

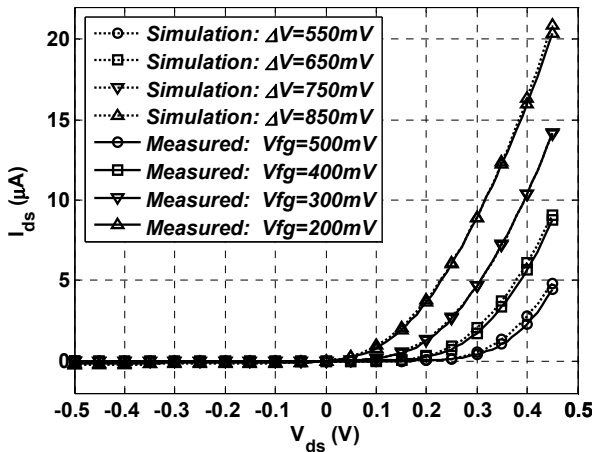


Figure 4. DC Characteristics of FGTD with different thresholds.

1. Initially inject all the FGTD to an ultra-low threshold using indirect programming. In this state the dc response between the input and the output of the charge-pump is equivalent to a closed switch.
2. Program the first FGTD in the charge-pump by using FN tunneling and at the same time measuring the dc current flowing between the input and the output terminal of the charge-pump. Stop the programming when the forward current becomes equal to a pre-determined value for a target input voltage (For our experiments, we chose 100nA for 300mV input voltages). Measure the I-V characters between the input/output terminals of the charge-pump to verify the operation of the structure as a single diode.
3. Program the second diode using its FN tunneling node such that the predetermined current level is achieved now at twice the input voltage (For our experiments this is equivalent to 100nA at 600mV).
4. Repeat step number 3 for all the diodes and at each step program the target current level at  $N$  times the input voltage, where  $N$  is the series count of the diode being programmed.

The above procedure obviates isolating each of the FGTD from the charge-pump circuit and using repeated injection and tunneling to equalize their threshold voltages. Figure 6 shows the I-V characteristics obtained at each programming stage where it can be seen that the pre-determined current of 100nA is reached for 300mV, 600mV, 900mV, 1.2V and 1.5V.

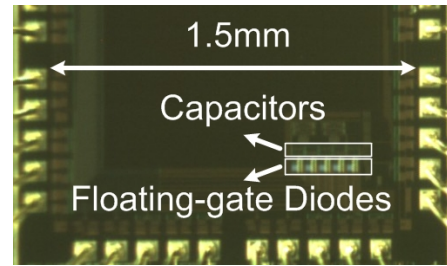


Figure 5. Micrograph of the prototype.

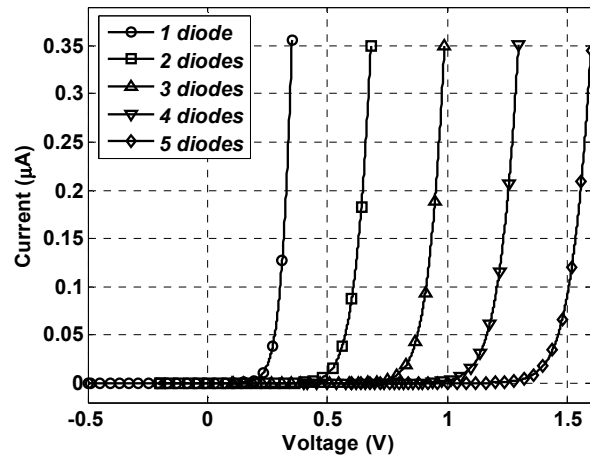


Figure 6. Initialization procedure for the FGTD charge-pump.

### B. Performance of the Charge-pump

A 5-stage voltage-multiplier charge-pump was initialized using the procedure described in section III.A and its AC response was measured. The amplitude of the input RF signal was set to 300mV which is below the threshold of the transistor of the 0.5- $\mu\text{m}$  CMOS process. The frequency of the input signal is swept from 0.1 MHz to 11 MHz and the output DC voltage was measured under no-load conditions. The measured characteristics are shown in Fig. 7 with the y-axis representing the voltage-gain (output dc amplitude/input ac amplitude) that can be obtained. The charge-pump provides a gain of approximately 2 which matches the theoretical performance of a 5-stage multiplier with the parameter  $\alpha \approx 0.5$ . The DC output is stable over the frequency range 1-4 MHz, which falls within the frequency band that has been shown to have good propagation characteristics through the human body [1][3].

Since the 1pF loading capacitor chosen for this prototype is not large enough, the charge sharing between each stage will achieve  $\alpha = 0.5$  in equation (1). Thus an ideal output gain is 2.5 for the 5-stage charge-pump which is close to the measured result shown in Fig. 7. The DC output is determined by the forward charging current and the reverse leakage current of the FGTD. Since the leakage current can be considered to be constant, there are more charges can be stored onto the load capacitors when the frequency of the input signal is increasing, which results in an increment in the magnitude of the DC output. However, the forward charging current will stop increase due to the limited response speed of the FGTD. Thus the DC output will drop gradually after reaching its peak.

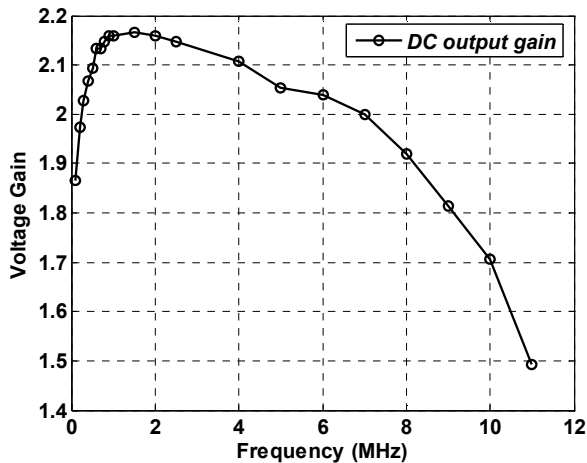


Figure 7. Frequency response of the output DC level.

### IV. CONCLUSION

This paper presents a novel structure of the charge-pump circuit using floating-gate transistors. The charge-pump using FGTD can harvest power from input signal as low as 50mV which is lower than the threshold voltage of a typical transistor. With the initialization procedure proposed in this paper, the charge-pump is capable of programming the threshold of all the FGTD offline using a small number of programming pads and is independent of process related artifacts. The charge-pump requires no additional compensation circuit, which is suitable for the power harvesting for the implantable sensors.

### REFERENCES

- [1] G. Iyengar, "A tour through the interaction between humans and electromagnetic spectrum," MIT Media Laboratory, Physics of Information Technology, 1996.
- [2] P. Vaillancourt, et. al, "EM radiation behavior upon biological tissues in a radio-frequency power transfer link for a cortical visual implant," 19th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, vol. 6, 1997, pp. 2499 – 2502.
- [3] F. Kocer, P.M. Walsh and M.P. Flynn, "Wireless, remotely powered telemetry in 0.25  $\mu\text{m}$  CMOS," Radio Frequency Integrated Circuits (RFIC) Symposium, 2004, pp. 339 – 342.
- [4] N. Tran, B. Lee and J.W. Lee, "Development of long-range UHF-band RFID tag chip using Schottky diodes in standard CMOS technology," Radio Frequency Integrated Circuits (RFIC) Symposium, 2007, pp. 281 – 284.
- [5] X. Wang, B. Jiang, W. Che, N. Yan and H. Min, "A high efficiency AC-DC charge pump using feedback compensation technique," IEEE Asian Solid-State Circuits Conference, 2007, pp. 252 – 255.
- [6] S. Mandal, R. Sarpeshkar, "Low-power CMOS rectifier design for RFID applications," IEEE Transactions on Circuits and Systems, vol. 54, no. 6, 2007, pp.1177 – 1188.
- [7] T. Le, K. Mayaram and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensors networks," IEEE Journal of Solid-State Circuits, vol. 43, no. 5, 2008, pp. 1287 – 1302.
- [8] E. Vittoz, J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," IEEE Journal of Solid-State Circuits, vol. 12, no. 3, 1977, pp. 224 – 231.
- [9] P. Hasler, "Foundations of learning in analog VLSI," Ph.D. Thesis, California Institute of Technology, Pasadena, 1997.
- [10] C. Diorio, P. Hasler, B. Minch and C.A. Mead, "A single-transistor silicon synapse," IEEE Transactions on Electron Devices, vol. 43, no. 11, 1996, pp. 1972 – 1980.
- [11] D.W. Graham, E. Farquhar, B. Degnan, C. Gordon and P. Hasler, "Indirect programming of floating-gate transistors," IEEE Transactions on Circuits and Systems, vol. 54, no. 5, 2007, pp. 951 – 963.